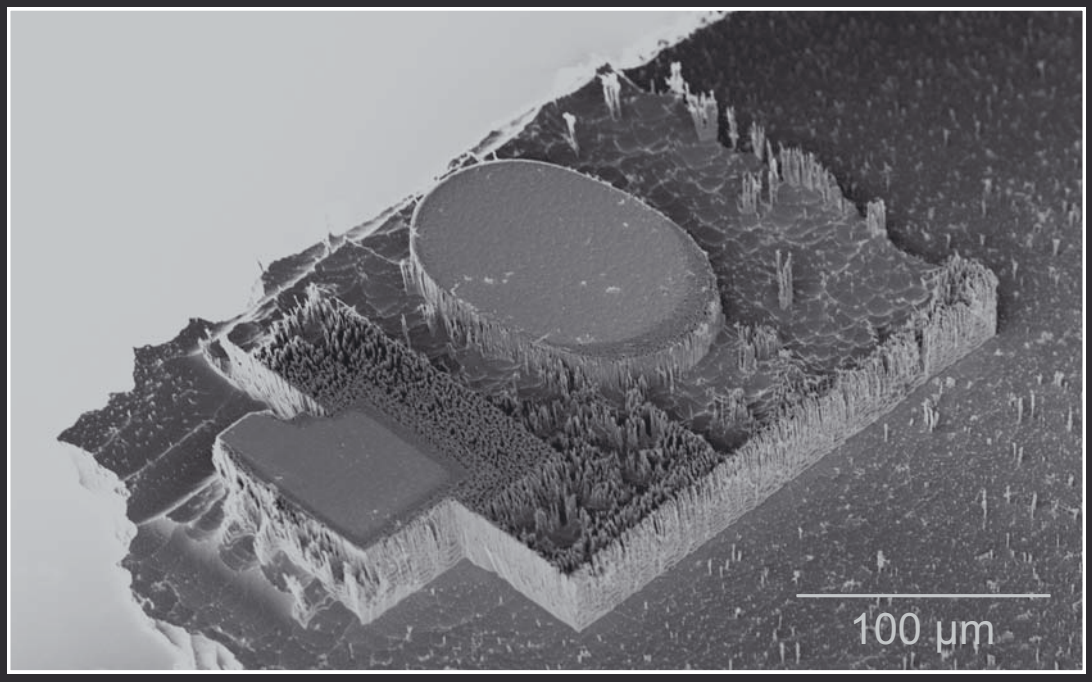
Fabrication process development for silicon micro and nanosystems

Nikolai Chekurov



Aalto University

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Nikolai Chekurov

Doctoral dissertation for the degree of Doctor of Science in Technology to be presented with due permission of the School of Electrical Engineering for public examination and debate in Auditorium AS1 at the Aalto University (Espoo, Finland) on the 25th of November 2011 at 12 noon.

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The image on the front cover is the electron microscope micrograph which became the starting point and the foundation of this thesis. It illustrates the masking capability of focused ion beam implanted gallium against cryogenic deep reactive ion etching. Sufficiently protected parts of a silicon chip are high and flat, while the rest of the area has been etched down partly or fully, depending on a doping concentration.

Aalto University

Abstract

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Abstract

Micromechanical devices have been fabricated out of silicon for decades, but only recently even smaller structures - nanodevices have become experimentally possible. Traditionally silicon devices are fabricated using separate lithography and various etching methods.

This thesis work concentrates on developing fabrication techniques for silicon micro and nanostructures. The goal was to achieve nanometer-scale feature size and simultaneously significantly speed up the most time consuming phases. For testing purposes also functional devices were designed and fabricated.

Main discoveries are related to the use of ion beam writing in a nonstandard manner. Instead of direct milling, methods were developed to directly use the beam to replace time consuming lithography step by the substrate treatment by ions. As a result, several silicon-based fabrication techniques were developed that require only a few processing steps and therefore can be realized in less than one day. The main achievement is in overcoming some of the limitations of serial writing methods such as those required in electron beam lithography or focused ion beam processing. High aspect ratio (laterally small, but tall) structures were successfully obtained using both technologies for the pattern transfer.

Fabrication techniques, described in this thesis, open up an opportunity for the developers to almost instantly test their ideas using functional components by altering the way nanosystems are developed. The presented methods cannot easily be extended to mass production but are appropriate in basic research and prototyping.

Keywords Silicon, Microfabrication, Nanofabrication, Focused Ion Beam, Deep Reactive Ion Etching

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Tiivistelmä
Piistä valmistettuja mikrorakenteita on pystytty valmistamaan jo vuosikymmeniä, mutta vasta viime aikoina on ollut mahdollista saada käytännössä tehtyä pienempiä rakenteita -nanosysteemejä. Perinteisesti piikomponentteja on valmistettu käyttäen erillistä litografiaa ja monenlaisia etsausmenetelmiä.

Väitöskirjassa keskitytään mikro- ja nanorakenteiden valmistusmenetelmien kehittämiseen. Tavoitteena oli saavuttaa nanometriluokan tarkkuus ja samalla huomattavasti nopeuttaa eniten aikaa vieviä työvaiheita. Menetelmien toimivuuden varmistamiseksi on myös suunniteltu ja valmistettu toiminnallisia komponentteja.

Työn tuloksena on kehitetty useita piipohjaisia valmistusmenetelmiä, jotka vaativat vain muutamia prosessivaiheita ja ovat toteutettavissa alle vuorokauden kuluessa. Työn pääpainopiste on sarjakirjoitusmenetelmien: elektronisuihkulitografian ja kohdistetun ionisuihkun hyödyntämisessä ja niiden rajoituksien kiertämisessä. Suuren aspektisuhteen (pieniä mutta korkeita) rakenteita on onnistuneesti valmistettu käyttäen kumpaakin menetelmää kuviointiin. Merkittävimmät kokeelliset uudet oivallukset liittyvät juuri ionisuihkukirjoituksen käyttöön hyvin ei-standardilla tavalla. Sen sijaan, että ionisuihkua käytettäisiin näytteen materiaalin leikkaamiseen tai poistamiseen, tässä työssä on sovellettu ionisuihkua korvaamaan koko litografiavaihe näytteen pintakäsittelyllä.

Väitöskirjassa kuvatut valmistusmenetelmät antavat mahdollisuuden kokeilla suunnitellun komponentin toimivuutta lähes välittömästi. Esitetyt menetelmät eivät ole helposti laajennettavissa massatuotantoon, mutta sopivat erinomaisesti perustutkimukseen ja prototyyppien valmistukseen.

Avainsanat Pii, mikrovalmistus, nanovalmistus, kohdistettu ionisuihku, syväetsaus
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Preface

The work presented in this dissertation was started at the beginning of 2006 at the Helsinki University of Technology, Micro and Nanosciences Laboratory and it was brought to the end in 2011 at a newly formed Aalto University, Department of Micro and Nanosciences. I would never get this far without the help of dozens of people I met during my time as a postgraduate student and I'm very grateful to everyone who contributed to this work.

First of all, I want to thank Professor Ilkka Tittonen who acted as a supervisor of this thesis, but more importantly, guided my academical progress for more than ten years and significantly influenced my whole life. I'm also grateful to Professor Sami Franssila for extensive support during the preparation of the FIB related publications and for generating a vast amount of ideas which sometimes turned into scientific publications and sometimes made it into the newspapers. Professor Jukka Pekola is acknowledged for giving me an opportunity to join his group for one of their really cool and fruitful experiments. I'm also thankful to the head of the department, Professor Kari Halonen, who greatly facilitated my studies during the last two years as a postgraduate. Special thanks to the director of the Aalto Nanofab, Veli-Matti Airaksinen, for his fair and consistent way of running things at Micronova.

I'm truly grateful to Kestas Grigoras, Victor Ovchinnikov, Aleksander Savin and Andriy Shevchenko - senior researchers I had a pleasure to work with. They patiently answered thousands of stupid questions and taught me a lot of practical things related to the study and to the life in general. I'm also indebted to Mika Koskenvuori who acted as an instructor in the beginning of this work and provided excellent ideas which kick-started my microsystem fabrication research. I thank Päivi Sievilä for introducing the world of experimental microfabrication and for the valuable peer support. I would also like to thank Sergei Kafanov who revealed to me the true meaning of the words "devoted scientist" and instructed the most ambitious project I have ever attempted. My acknowledgments to Pasi Kostamo, Kimmo Kokkonen and Antti J. Niskanen for demonstrating a level of expertise worth admiring and trying to reach for.

I'd like to acknowledge all the co-authors of the publications I have been a part of; Lauri Sainieimi, Ossi Hahtela, Antti Peltonen and Khattiya Chalapat among others. I really enjoyed working with you and hope we will become colleagues again some day.

I want to thank the staff of Micronova, especially Paula Heikkilä, for doing an excellent job on keeping the place running and for your countless solutions to all the problems I bothered you with. I also thank Aila Blomberg, whose skills and

persistence in the field of public relations got me several lifetimes worth of media attention.

I thank the people with whom we spent a lot of time doing the evening shifts, fixing equipment or just complaining about the injustice of the world; Markus Bosund, Jakub Gronicz, Wonjae Kim, Ossi Kimmelma, Ville Maisi, Marco Mattila, Päivi Mattila, Matthias Meschke, Juha Muhonen, Ville Pale, Joonas Peltonen, Olli-Pentti Saira, Maksim Shpak, Antti Säynätjoki, Andrey Timofeev, Aapo Varpula and Osmo Vänskä.

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Finally, I want to thank my family and friends for their irreplaceable support and encouragement during all those years.

Helsinki, November 2011

Nikolai Chekurov

Contents

List of Publications

This thesis consists of an overview and of the following publications which are referred to in the text by their Roman numerals.

I O. Hahtela, N. Chekurov and I Tittonen, "Non-tilting out-of-plane mode high-Q mechanical silicon oscillator", *Journal of Micromechanics and Microengineering*, **15**, 1848-1853 (2005).

II N. Chekurov, M. Koskenvuori, V-M. Airaksinen and I. Tittonen, "Atomic layer deposition enhanced rapid dry fabrication of micromechanical devices with cryogenic deep reactive ion etching", *Journal of Micromechanics and Microengineering*, **17**, 1731-1736 (2007).

III N. Chekurov, K. Grigoras, A. Peltonen, S. Franssila and I. Tittonen, "Fabrication of Silicon Nanostructures by Local Gallium Implantation and Cryogenic Deep Reactive Ion Etching", *Nanotechnology*, **20**, 065307, (2009).

IV N. Chekurov, K. Grigoras, A. Peltonen, S. Franssila and I. Tittonen, "Localized Gallium Doping and Cryogenic Deep Reactice Ion Etching in Fabrication of Silicon Nanostructures" Ion Beams and Nano-Engineering, edited by D. Ila, P.K. Chu, N. Kishimoto, J.K.N. Lindner, J. Baglin (Mater. Res. Soc. Symp. Proc. Volume 1181, Warrendale, PA, 2009), 1181-DD07-0.

V N. Chekurov, K. Grigoras, L. Sainiemi, A. Peltonen, I Tittonen and S Franssila, "Dry fabrication of microdevices by the combination of focused ion beam and cryogenic deep reactive ion etching", *Journal of Micromechanics and Microengineering*, **20**, 085009 (2010).

VI P. Sievilä, N. Chekurov, I. and Tittonen, "The fabrication of silicon nanostructures by focused-ion-beam implantation and TMAH wet etching", *Nanotechnology*, **21**, 145301, (2010).

VII J. P. Pekola, V. F. Maisi, S. Kafanov, N. Chekurov, A. Kemppinen, Yu. A. Pashkin, O.-P. Saira, M. Möttönen, and J. S. Tsai, "Environment-Assisted Tunneling as an Origin of the Dynes Density of States", *Physical Review Letters*, **105**, 026803 (2010).

Author's contribution

Publication I:

The author has performed design and optimization of silicon resonators by means of simulation utilizing commercial software. Fabrication and characterization were performed by co-authors.

Publication II:

The author participated in developed the fabrication technique, fabricated the samples and participating in manuscript writing. Component design and characterization were performed by co-authors.

Publications III, IV:

The author discovered the fabrication technique and carried out the experiments. Planning experiments, analyzing results and writing the manuscript was performed in collaboration with co-authors.

Publication V:

The author participated in planning the experiments, carried out resonator fabrication and thermal actuator modification. Measurements and data analysis as well as writing the manuscript were performed with co-authors.

Publication VI:

The author presented the original idea, participated in planning and carrying out the experiments. The author participated in result analysis and manuscript writing.

Publication VII:

The author fabricated shielded substrates used in experiments.

List of Abbreviations

ACE	Acetone
AFM	Atomic Force Microscope
ALD	Atomic Layer Deposition
BOX	Buried Oxide
CCP	Capacitively Coupled Plasma
CMOS	Complementary Metal Oxide Semiconductor
CVD	Chemical Vapor Deposition
DETF	Double-Ended Tuning Fork
DRIE	Deep Reactive Ion Etching
EBL	Electron Beam Lithography
FEM	Finite Element Modeling
FIB	Focused Ion Beam
FWHM	Full Width at Half Maximum
HF	Hydrofluoric Acid
IC	Integrated Circuit
ICP	Inductively Coupled Plasma
IPA	Isopropanol
KOH	Potassium Hydroxide
LMIS	Liquid Metal Ion Source
MEMS	Microelectromechanical Systems
NEMS	Nanoelectromechanical Systems
NIS	Metal-Insulator-Superconductor
PECVD	Plasma Enhanced Chemical Vapor Deposition
PMMA	Poly(methyl methacrylate)
RF	Radio Frequency
RIE	Reactive Ion Etching
SEM	Scanning Electron Microscope
SINIS	Superconductor-Insulator-Metal-Insulator-Superconductor
SOI	Silicon On Insulator
TEM	Transmission Electron Microscope
TMA	Trimethylaluminium
TMAH	Tetramethyl Ammonium Hydroxide ((CH3)4NOH)

1 Introduction

Micromachining of silicon relies heavily on existing microelectronics fabrication technologies. There is a huge delay between the time when new technology is applied to the integrated circuit production lines and when it becomes available for the micromachining purposes. At the end of 2010 there are ICs in production with the half-pitch of only 22 nm and at the same time fabrication of the mechanical silicon components is restricted in resolution to 2 µm – 3 µm. The reason for such a gap is in highly different requirements for the IC and micromechanical processes. When in electronics the patterned surface can be assumed to be planar and the vertical dimensions of resolution-critical layers are in tens of nanometers, mechanical structures require that fabrication steps could create the height differences of several microns.

Many methods have been proposed to enhance the available resolution, but there are two main approaches: top-down and bottom-up. Bottom-up techniques are based on simple blocks which self-organize in complex structures. They can cover huge areas and can produce shapes as small as few nm, but their weakness is a tendency to produce random defects, which is not tolerable in many cases.

The top-down approach is represented by various lithography techniques, where the pattern is designed as a whole first and then transferred to the structures. This method works well when the predetermined arbitrary shapes are required but it has strict limitations on the minimum resolution as well as issues in combining high (nm) resolution writing with large (mm) writing area.

Unlike in IC industry, where the fabrication processes are fixed and documented to a point, where the whole electronic circuit can be simulated with great accuracy already at the design stage, for most MEMS/NEMS(micro/nano-electromechanical systems) the required fabrication process must be tailored every time without meeting the possibility to use any standard clean room process on external foundry.

When using standard photolithography masks, even mass production becomes possible but designing and creating a physical mask is time consuming. One solution is to replace photolithography with serial writing methods. There are several such methods available, but only two of them can reach the nanoscale resolutions, namely electron beam lithography (EBL) and focused ion beam (FIB). By using one of these methods, a design is transferred to the machine electronically and written/processed directly on the component. The downsides are quite a slow speed and small writing area, so processing of structures with side length > 1 mm becomes difficult. EBL resists are also usually quite thin and can not provide enough masking in prolonged etches. FIB milling time depends on the volume of material removed, rather than the area, so processing time is cubically scaled to a feature size.

The objectives of this thesis is to develop fabrication techniques, which are capable to produce silicon structures, or even complete microsystems with precision better than 100 nm without the need for using a physical mask. The developed processes are used in fabrication of functional components, such as radio frequency micro-electro-mechanical systems and thermal actuators. The great benefit and interesting practical result is that the developed processes can be realized in a few hours starting from the design.

In this work, in transferring the original design only maskless patterning techniques (EBL and FIB) were employed to avoid relatively slow process of producing photolithographic masks. Patterned components were fabricated using cryogenic deep reactive ion etching technique (DRIE) or by wet etching in tetramethylammonium hydroxide (TMAH). Both of the methods etch silicon at a rate of > 0.5 µm/min, which is more than sufficient for the purpose of producing nano-sized structures.

This thesis focuses on the fabrication techniques, their development and characterization, rather than on final applications. As a result of the work, several micro and nanofabrication techniques which can produce functional micro- and nanosystems were developed.

Seven publications are included in this thesis: In publication I a silicon micromachined resonator vibrating in non-tilting out-of-plane mode is designed and characterized. In publication II a novel approach on prototyping radio frequency (RF) MEMS using EBL, DRIE and atomic layer deposition (ALD) is demonstrated. Publication III shows a novel masking method for cryogenic DRIE which utilizes a thin Ga^+ doped layer created by FIB. Publication VI extends this method to TMAH wet etching. Publications IV and V describe the use of a combined FIB and DRIE technique for creating thin free-standing structures, nanowires and released microsystems. Finally the publication VII describes the environment modification for mesoscopic conductors such as tunnel junctions.

2 Common fabrication techniques

Micro- and nanomachining is way too delicate to use mechanical tools such as drill bits or milling cutters, so other means such as ion milling or chemical etching are employed. The workpiece, which is usually a polished wafer or a plate, is first protected by a patterned layer, and then its whole surface is processed so all the unprotected areas are machined away.

The protective layer is usually a light sensitive polymer photoresist, which can be exposed with a desired pattern and developed. In this process called photolithography the resists solubility in developer changes depending on if it has been lit or not. By the means of photolithography photoresist can be patterned with an accuracy much better than 1 µm.

Sometimes the protective capabilities of polymers are not sufficient for longer and deeper etches, or polymer masks can not be used. In those cases a thin layer of material which is resistant to etchants is deposited before patterning and etching is performed in two steps, first the thin masking layer is patterned forming a hard mask and then the actual processing is done using that mask.

This chapter reviews fabrication steps mentioned above, namely patterning, masking and etching for fabricating various nano and microsystems.

2.1 Patterning

Creating mechanical devices with the smallest feature size below 1 µm requires the use of advanced patterning techniques. A traditional solution is photolithography, but it has its limitations, such as the Rayleigh resolution limit at the wavelength of the light used for the projection (currently $\lambda = 193$ nm). There are also extremely strict requirements on flatness of the patterned surface, as the depth of focus of the projection system is in the same range as the wavelength of the light used [1]. Nanoimprint lithography can tolerate the surface undulations [2], and can achieve very high resolution [3], but being a strictly mass-production method it can not be easily employed when only a few components are needed. One common aspect of both methods is a need for an original photolithographic mask or a stamp master. Production of such a mask is a slow process which requires its own, usually external fabrication facility.

There are several approaches, which can allow maskless lithography, such as the interference image patterning or self-assembly based schemes. While having the possibility to choose the resulting pattern from a wide variety of predetermined shapes, those methods can not always provide arbitrary shape or inter-layer alignment. [4]

In this work the focus is on serial writing techniques, in which the pattern is written with a single beam forming one pixel at a time. There are optical tools which rely on scanning laser beams or optical reduction of shapes formed by blades. Such tools suffer from the same resolution restrictions as the conventional photolithography tools. The techniques which reach the true nanoscale resolution are electron beam lithography (EBL), focused ion beam (FIB) lithography, and scanning probe lithography as none of them uses light for writing. While EBL is widely used for photolithographic mask fabrication, the use of FIB is rather new since the appropriate technology has been developed quite recently [5]. Scanning probe lithography despite is still an experimental technique as the resulting throughput is extremely low even when compared with other serial writing tools [6]. The slow writing speed and a small writable area of EBL and FIB do not allow to use them directly in production, but in this work it is shown that when only prototyping is concerned, those restrictions do not constitute a serious problem.

2.1.1 Electron Beam Lithography

Electron beam lithography is one of the most commonly used techniques when the resolution beyond the optical limits is required [7]. The method is based on the electron beam instead of light rays for producing images or exposing the sample. The operating principle of scanning electron microscope (SEM) is in shining the area of interest on a sample with a narrow electron beam and consequently detecting the emitted electrons, forming an image pixel-by-pixel.

The minimum electron beam diameter which directly affects the resolution of the SEM is limited by the size of electron source, aberrations in optics and diffraction. The wavelength of the electron accelerated with a typical energy in the range between 5 keV and 100 keV is from 17 pm down to 3.7 pm, but even then the classical diffraction effects may occur when very high resolution systems are considered [5]. At the end of 2010, the resolution of high-end commercial SEM is generally better than 1 nm and can in some special cases be as high as 0.4 nm [8].

Usually the application of EBL requires polymer resist to be used [5]. In the positive resists, the electron exposure breaks the polymer chains, making them soluble in a developer and in the case of the negative resist, cross linking occurs upon exposure, rendering the exposed parts non-soluble. There is a vast variety of possible resists starting from a fairly common PMMA or ZEP to exotic non-polymer resists. Resists play also an important role in reaching the resolution that is below 10 nm.

An electron microscope can be converted to an EBL machine by adding an external pattern generator which takes control of the beam deflection and blanking as well as of the stage movement. In this way, the electron beam can be used to write patterns defined by an electronic design (Figure 2.1).

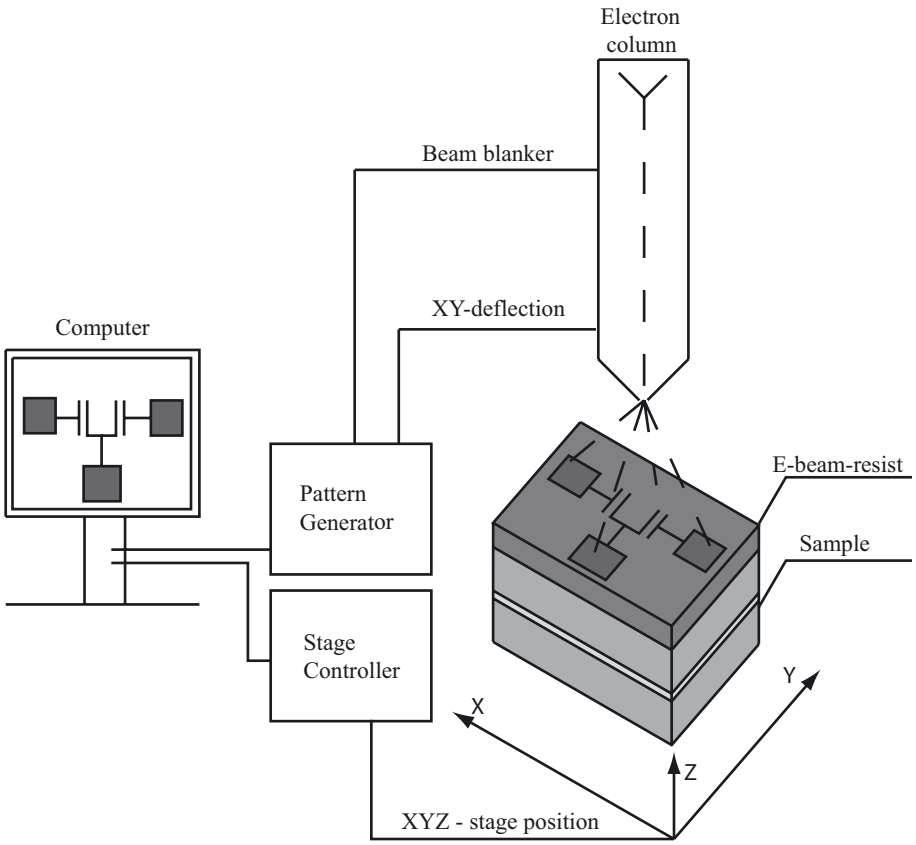

Figure 2.1: EBL block diagram. The design is created electronically and transfered by the control computer to a pattern generator, which controls the XY-deflection of the beam in column and the beam blanker (if available). There is also a possibility to control the mechanical stage to make several exposures on a sample. The final pattern is formed by the electron beam on a photoresist.

While with EBL one can achieve very high resolution, there are also various technical challenges. The field of view of a SEM, or a dedicated EBL machine is usually at the order of 1 mm, so larger patterns have to be split into smaller blocks, which are written separately to several different positions. This arises stitching issues at the boundaries of the writefields, as no mechanical stage is perfect and even the interferometric stages in which systems position is determined in a closed loop, cause some error in positioning. EBL brings along low throughput, which limits its industrial use to photolithography mask fabrication.

2.1.2 Focused Ion Beam processing

The operating principle of the focused ion beam (FIB) resembles that of the scanning electron microscope. The natural difference is that instead of exposing the surface of the sample with electron beam, an ion beam is applied. The most common ion source for FIB is a liquid metal ion source (LMIS) of which gallium ion source is the most widespread one [9]. Because ions are much heavier than electrons ($m_{Ga} = 10^{-28}$ kg, wavelength at typical acceleration voltages is in the range $\lambda = 0.5 - 2$ pm), they induce sputtering which enables direct modification of samples (Figure 2.2).

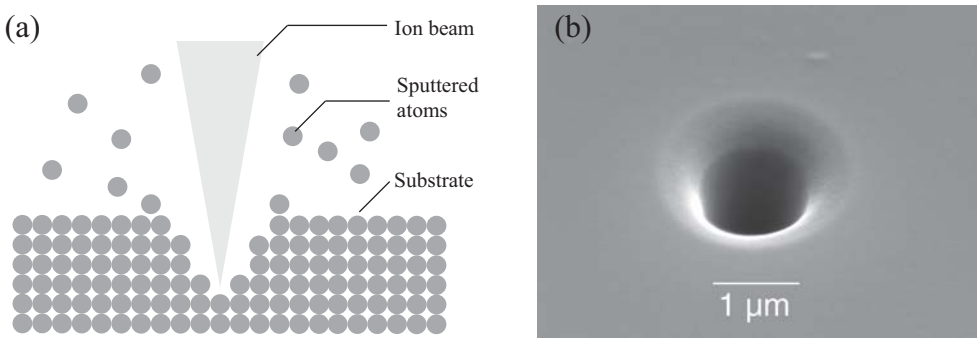

Figure 2.2: FIB sputtering. (a) schematic representation, (b) a hole milled in silicon as a result of a few second exposure with 9.3 nA 30 kEv Ga^+ beam indicating the order of magnitude of the beam diameter.

The smallest achievable beam diameter depends on the beam current and the acceleration voltage. The resolution of ion beam is limited by similar factors as in a case of an electron beam. In milling applications, the higher acceleration voltage corresponds to higher accuracy and sputtering efficiency, so usually the maximum available acceleration voltage is appropriate. When the damage to the sample surface is an issue, as is the case in the sample preparation for transmission electron microscopy (TEM), lower acceleration voltages can be used to minimize the amorfization of the milled structure.

Beam current governs directly the beam diameter, so the smallest current can produce the finest spot. Figure 2.3 shows such a dependence for FEI Helios NanoLab 600 machine using 30 kV acceleration voltage. The spot diameter refers here to a full width at half maximum (FWHM) value of the beam that is assumed to have a Gaussian profile. The sputtering rate is directly proportional to the beam current, so there is a trade-off between the accuracy and milling speed.

In order for the sputtering effect to appear, a certain amount of ions have to be delivered to the sample surface. This amount can be determined by a simple formula:

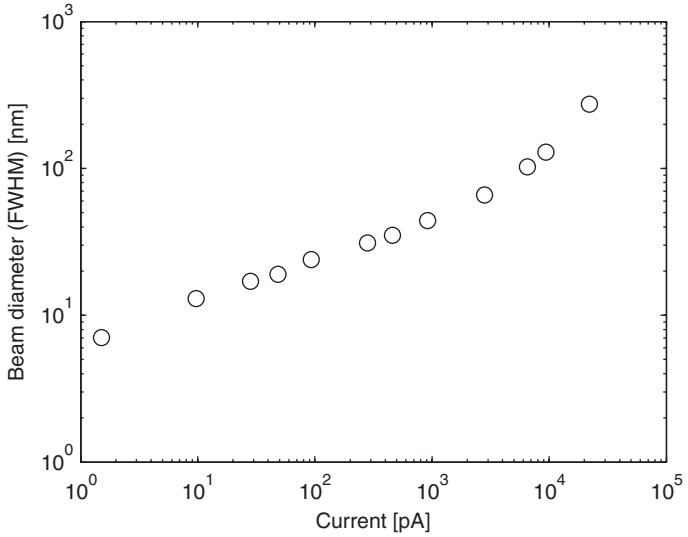

Figure 2.3: Ion beam diameter as a function of the beam current for Helios Nanolab 600 machine as specified by manufacturer. The real diameter is somewhat bigger than indicated here due to non ideal focusing.

$$Dose = \frac{i \times t}{A \times q}, \tag{2.1}$$

where i is the beam current on a sample, t is the irradiation time, A is the irradiated area and q is the charge of a single ion. For Ga^+ ions q is the same as the electron charge $e = 1.6 \times 10^{-19}$ C.

To achieve deep 3D structures requires ion doses around 10^{18} cm^{-2}, which is usually not feasible, as it involves a current or an exposure time to be disproportionally high. To address this issue, FIB assisted etching techniques have been developed. In case of silicon the use of Cl_2, Br_2 or I_2 can amplify the sputtering yield and speed-up the processing by a factor of 8 at best [10]. Figure 2.4 shows a pillar structure fabricated using FIB assisted etching. It took about 2 hours to remove less than 15 µm^3 of silicon with a beam current of 10 pA.

Even in the case of FIB enhanced etching, the processing time is usually too long for creating structures directly from silicon wafer, so FIB is mainly used for amending pre-fabricated structures and microanalysis. Figure 2.5 shows the result of narrowing a predefined silicon bridge by an FIB. The width of a 4 µm thick bridge was decreased from 7.5 µm to 5 µm over a distance of 100 µm. 1000 µm^3 of silicon were removed in 25 minutes with a high-current beam of 19 nA and then the wall quality was improved by polishing with a current of 7.9 nA for 10 minutes.

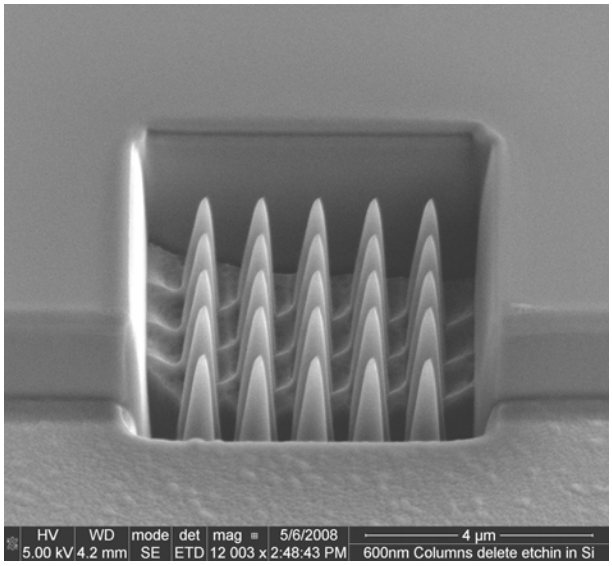

Figure 2.4: Silicon pillar array fabricated using FIB assisted etching. The processing time was 106 min. (Picture courtesy of Antti Peltonen, Aalto University.)

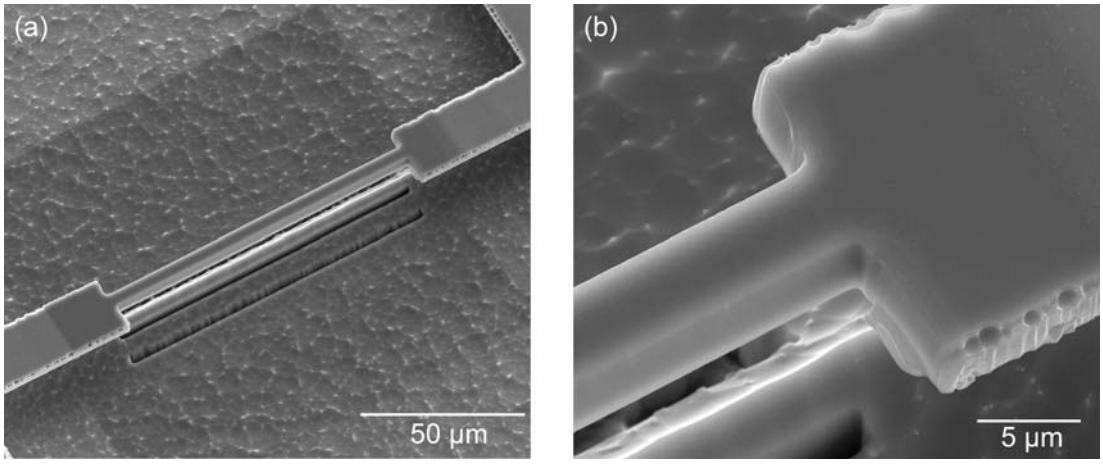

Figure 2.5: Modification of the pre-fabricated free-standing silicon bridges. (a) overview on a narrowed bridge, (b) close-up showing the resulting wall quality.

One way to bring FIB closer to the speed performance of EBL is to utilize its property of doping the substrate with the ion beam material. In case of a silicon substrate and gallium ion bombardment, the distribution of ions is shown in Figure 2.6. The distributions were calculating using the SRIM simulation software [11]. Figure 2.6(a) shows the schematic representation of simultaneous milling and dop-

ing. Figures 2.6(b) and 2.6(c) illustrate the depth distribution of 30 keV gallium ions in silicon substrate as well as the lateral distribution. The penetration depth (range) of the Ga^+ ions in silicon is 28 nm with a standard deviation of 10 nm. The lateral distribution is between 4 and 10 nm depending on the implantation depth so, in theory, structures down to 20 nm in size can be written. In practice, the ion beam is not perfectly focused to a single spot and it's diameter limits the maximum achievable resolution in most cases to around 50 nm.

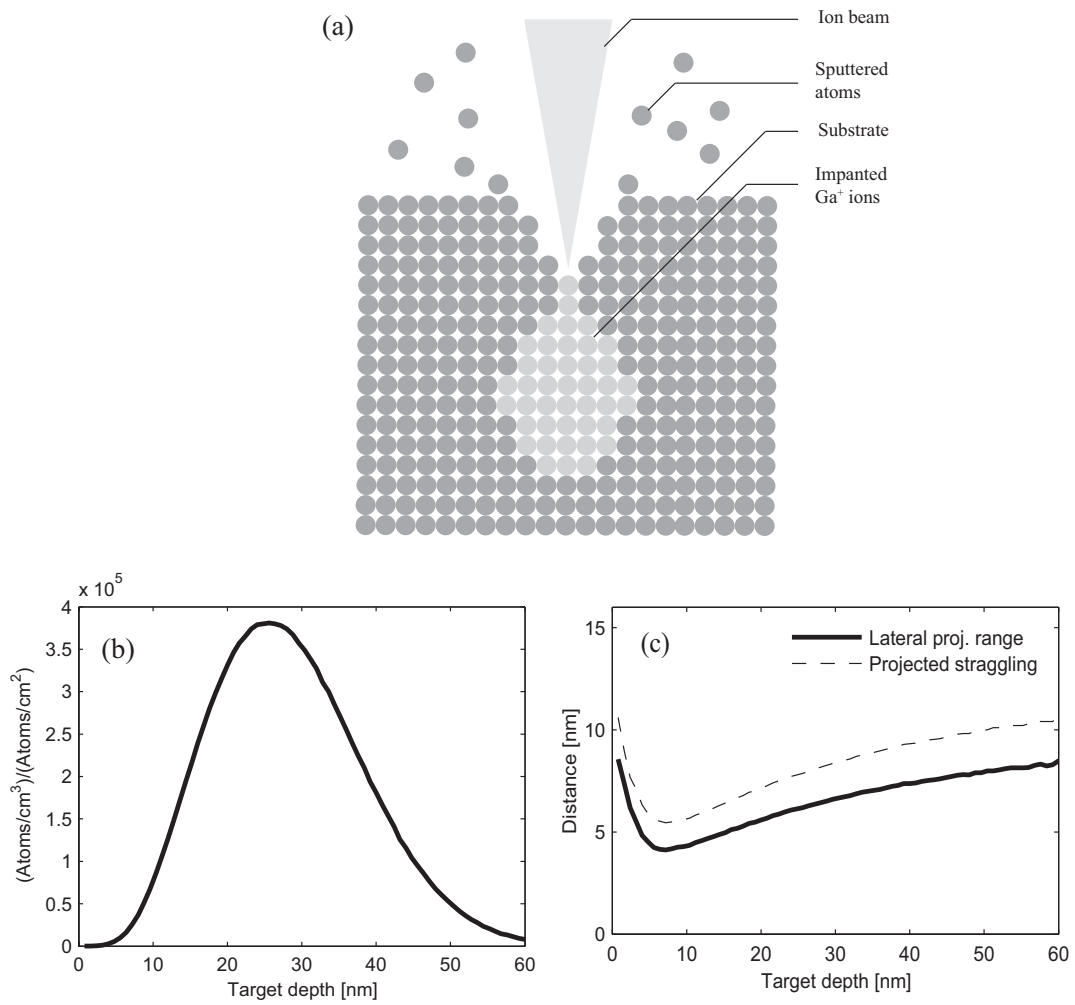

Figure 2.6: Gallium doping of silicon during FIB processing. (a) schematic representation of the doping profile. (b) Gallium ion depth distribution in silicon with the ion energy of $E = 30$ keV. (c) lateral distribution of gallium ions.

Doped regions of the sample exhibit different etching properties from the untreated ones, making it possible to utilize separate etching steps for actual removing of the material, minimizing the ion dose required. 2D patterning requires doses of 10^{12} – 10^{15} cm^{-2} for modification of a few nanometer thick surface layers [12], while

sputtering becomes evident at the doses above 10^{16} cm^{-2}.

Highly doped ($> 10^{19}$ ions cm^{-3}) silicon has for a long time been known to have a good resistance against certain wet etchants [13, 14]. The process of forming an etch-stop layer by introducing p-type dopants is routinely used in microfabrication [4]. Ga^+ ions implanted by FIB also are known to modify the etching properties of silicon [15] and many groups have utilized this property for micro- and nanostructure fabrication [16, 17, 18, 19], however all those works employ potassium hydroxide (KOH) for silicon etching. The Ga^+ doped silicon areas are also shown to dissolve to hydrofluoric acid (HF), enabling fabrication of concave structures [20].

The CMOS process compatible TMAH etchant was utilized together with Ga^+ FIB local doping for the first time in Publication VI of this thesis.

It has been shown [15] that Ga^+ doped silicon is also resistant towards dry etching in SF_6/O_2 plasma. Some work has been done towards developing this method as one possible micro- and nanostructure fabrication technique [21]. In publication III an exceptional resistance of gallium treated silicon in cryogenic DRIE (FIB/DRIE process) was demonstrated for the first time. This work was followed by similar results by another group [22], [23].

2.2 Masking

When the polymer resist layer durability is not sufficient to withstand prolonged etching, an extra layer between the substrate and resist is deposited. That thin layer is then patterned and serves as a hard mask as shown in Figure 2.7.

The requirements for the hard mask material are good selectivity in the main etching process and the ability to be etched through the photoresist mask. One of the most popular mask materials is silicon dioxide (SiO_2), which can be thermally grown on silicon, or deposited by chemical vapor deposition methods (CVD). The strength of the thermal oxide is its superior quality, but growing such an oxide requires the sample to be heated to approximately 1000 °C, which is not commonly applicable.

The CVD methods, especially PECVD (plasma enhanced chemical vapor deposition) provide a quick way to deposit mask films at moderate temperatures below 300 °C. The downside of PECVD is usually a poor quality of the end product, as pinholes can appear and the etch resistance towards wet etchants can be significantly weaker than in the case of using thermal oxide. Usually thermal annealing improves the film quality [24, 25], but the annealing is performed at temperatures comparable with the ones used in direct thermal oxidation.

Metallic films, such as those made out of aluminum, have extremely good selectivity

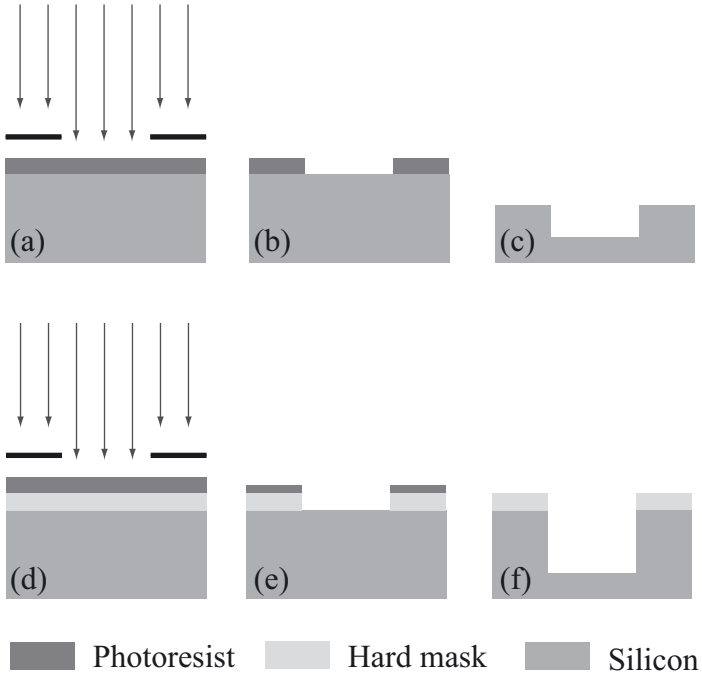

Figure 2.7: Etching process without (a-c) and with (d-f) a hard mask. (a) exposure, (b) development, (c) deep etching and resist failure leading to insufficient trench depth. (d) exposure of the resist above the hard mask, (e) patterning of the hard mask, (some resist is consumed) (f) deep etching through the hard mask. Because of a good etch resistance the hard mask is intact.

towards silicon in RIE applications, are quick to deposit using sputtering and in most cases easy to pattern with wet etchants. However, metallic masks are not suitable for the wet etching of silicon, as they tend to dissolve in silicon etching solutions or are extremely difficult to remove after the etching. Also using wet etching to pattern metallic layers sets restrictions on the smallest feature size, as the etching is isotropic.

Ceramic masking layers grown by atomic layer deposition (ALD) are able to combine the good qualities of metallic and non-metallic hard masks. ALD deposition of alumina Al_2O_3 can be performed at temperatures below 100 °C, and the resulting film is conformal and pin-hole free. Alumina is also found to have exceptionally high selectivity to silicon when cryogenic DRIE is concerned [26] so that even 4 nm thick layer is sufficient for most etching purposes. Depending on the resist material, patterning of the Al_2O_3 mask can be performed by using wet or dry etching.

2.3 Etching

Generally there are two ways to etch material, which are the wet etching where liquid chemicals are used and the dry etching [4]. The strengths of the wet etching are its low cost and straightforward batch processing. Wet etching works isotropically in amorphous or polycrystalline materials, which can limit its use in some cases, but in the case of crystalline silicon such wet etchants exist that result in considerable selectivity between crystal planes, making it possible to create various sidewall profiles by selecting the orientation of the substrate.

2.3.1 Wet Etching

As hard mask materials are almost always amorphous or polycrystalline, care must be taken in the use of wet etchants not to let the undercut of the mask over-widen the patterns (Figure 2.8).

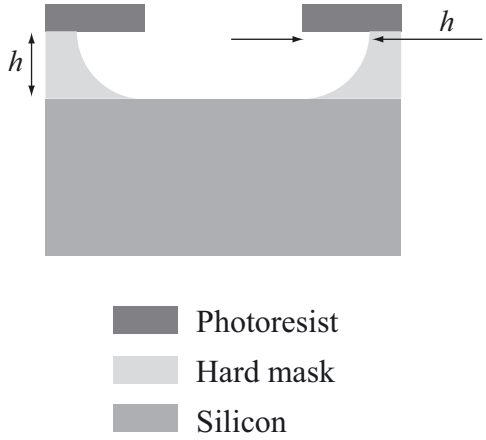

Figure 2.8: Effect of isotropic etching on the patterning accuracy. In this case the mask undercut is at least equal to the etched height.

For crystalline silicon, such wet etchants exist [27] that exhibit crystal plane selectivity. By choosing single crystal silicon substrates with proper orientation, anisotropic wet etching can be used to produce sloped or vertical wall profiles, as well as providing means for simple fabrication of suspended structures (Figure 2.9). Two common silicon wet etchans are potassium hydroxide (KOH) and tetramethyl ammonium hydroxide ($(CH_3)_4NOH$, TMAH) which are both used in aqueous solution. Both these etchants are well-characterized and widely used in micromachining [14, 27, 28, 29, 30, 31]. One important advantage of TMAH against KOH is the absence of metallic ions, making it compatible with CMOS processes, which allows its use within microelectronics fabrication facilities.

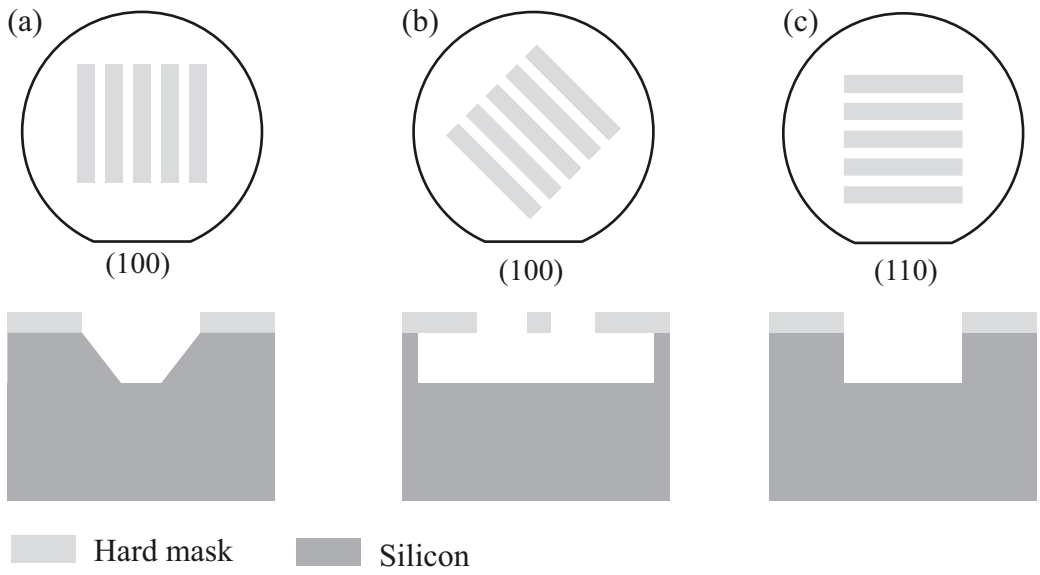

Figure 2.9: Crystallographic etching. The upper images show the orientation of the grooves on the wafer, the lower ones indicate the resulting etch profile. (a) sloped walls on (100) wafer, (b) etching with undercut on (100) wafer for the released structures, (c) vertical profile on (110) wafer.

If deep and narrow channels are produced using wet etching, care must be taken during drying of the sample, since the capillary effect (stiction) could easily cause collapsing of the structures. The problem is particularly serious in the case of released structures. [4]

2.3.2 Dry etching

In dry etching no liquids are present in the process as it is performed in a gaseous state. Usually the plasma is ignited in the reaction chamber to maintain the proper condition for etching, but the results can also be achieved without plasma [32]. The chemical process together with ion bombardment makes it possible to etch anisotropic wall profiles in amorphous or polycrystalline materials [4].

For silicon several dry etching methods and chemical processes exist, from simple argon sputtering in a capacitively coupled plasma [33, 34] to ultra-high speed multi-generator pulsed mode techniques [35]. This work concentrates on cryogenic DRIE out of possible dry etching processes.

The cryogenic DRIE etcher used in this work (Oxford Instruments Plasmalab 100) consists of two separate power sources that both operate at 13.56 MHz. Inductively

Gases	Temperature	Wall profile
SF_6/O_2	-120 °C	Vertical
SF_6	-120 °C	Crystallographic
SF_6	-80 °C	Isotropic

Table 2.1: Cryogenic DRIE etching modes.

coupled source (ICP) creates the high density plasma at typical power values in the range 600 W $> ICP_P >$ 2000 W. This plasma is then driven to the sample with a separate capacitively coupled generator with much less power in the range 2 W $> CCP_P >$ 10 W. A gas mixture of SF_6 and O_2 is used in proportion of 15 % to 17 % of oxygen. The substrate is kept at the temperature of -120 °C or -80 °C depending on the desired side wall profile. During the process silicon is etched by reactive ions from the high density plasma. The protective polymer layer forming occurs simultaneously, when the temperature of the substrate is less than c.a. -100 °C. Due to the ion bombardment induced by CCP, the polymer is etched away from horizontal surfaces while still protecting the vertical ones. [36, 37] A typical etch rate is c.a. 2 µm.

The resulting wall profile can be tailored by adjusting the gas mix ratio or changing the substrate temperature (Table 2.1). Often the most challenging thing is to create vertical walls, which is the reason why the mixture of SF_6 and O_2 ratio is of the highest importance, as it governs the polymer grow rate. If in this mixture the oxygen concentration is too low, the profile will become isotropic or crystallographic, as the vertical walls are not protected. If there is excessive oxygen, micromasking occurs and the etch rate falls rapidly [38].

The simplest case is the isotropic etching. As no passivation is required, pure SF_6 plasma is sufficient to produce required profile. For etching no cryogenic temperatures are needed, but in some cases they are desirable from the mask durability point of view.

Notching

Notching phenomena occur at the interface between silicon substrate and dielectric during plasma etching and is generally an unwanted underetching effect. This effect is usually observed while etching through the device layer of a SOI wafer. Non-conductive buried oxide becomes positively charged, and an electrical field is formed between the sidewalls and the bottom of the trench [39]. The incoming ions are deflected sideways from the charges in the bottom but etching still continues. Notching effect is highly dependent on the height to width ratio of the etched struc-

tures. Generally ratios $h/w < 1$ do not lead to noticeable notching [40] but the effect is significant when the aspect ratio grows (Figure 2.10).

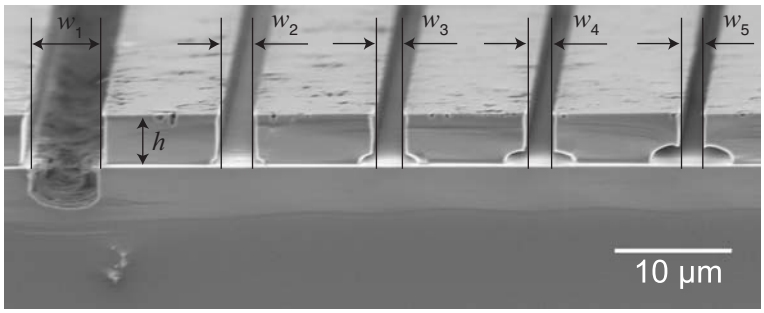

Figure 2.10: The dependence of the notching effect on the h/w aspect ratio. Structure height $h = 4$ µm, gap width is varied from left to right $w_1 = 5$ µm, $w_2 = 2$ µm, $w_3 = 1.7$ µm, $w_4 = 1.5$ µm, $w_5 = 1.2$ µm.

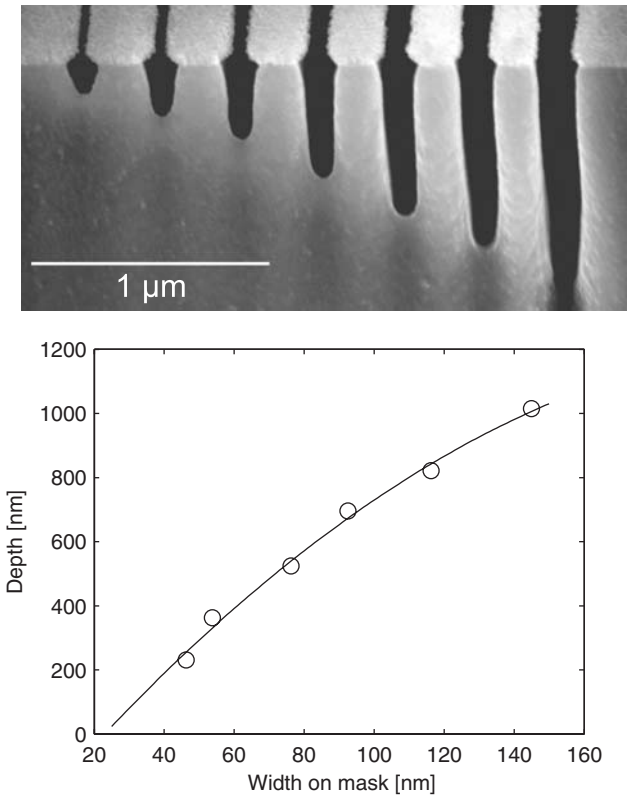

Figure 2.11: RIE lag illustration, the depth of the etched trenches is nonlinearly dependent on the width of the mask opening.

RIE lag

RIE lag refers to the effect where dry etching speed is decreased when high aspect-ratio structures are machined due to poor exchange of chemicals and radicals on the bottom of the etched structures. As a result, the depth of the trenches varies with their width when a series of gaps are produced on a single sample with the same etching time for all the structures. Figure 2.11 illustrates this negative effect.

3 Developed nanofabrication techniques

This chapter presents the main results achieved in this thesis concerning nanofabrication methods. Most results are novel and not published before this work.

3.1 Nanofabrication techniques

The main achievement of this study is the development and characterization of nanofabrication techniques which combine focused ion beam technology with various etching methods. Those combinations benefit both from the accuracy FIB provides and in the speed and the wall profile control the etching methods.

3.1.1 Patterning and etching of nanostructures

In Publications III and VI gallium doping was found to be able to modify the etching properties of single crystal silicon surface, making it extremely durable against cryogenic DRIE and TMAH. To characterize the promising masking method, two sets of different experiments were performed. The first approach was designed to determine the gallium dose requirement for various etching times and depths and the second one concentrated on finding the maximum achievable resolution.

Ga^+ doping dose for masking in cryogenic DRIE

The ion dose required for masking in cryogenic DRIE was measured by implanting a series of large patches (300×300 µm^2) using FEI Helios Nanolab 600 machine, which is capable of producing ion currents up to 21 nA. Large patches were selected, as they can easily be measured with a profilometer. The dose in the center of the patch does not depend on the beam shape as the beam diameter d is more than 1000 times smaller than the size of the patch.

Two sets of etching experiments were performed, one bearing in mind the microfabrication concentrating on smaller features (Figure 3.1(a)) and the second one for testing the limits of the masking capability (Figure 3.1(b)). The curves show the height of the resulting structures after etching. In those curves, the dose range from 5×10^{14} to 10^{17} ions cm^{-2} is covered with corresponding etching times from 1 to 40 minutes. The selectivity between the doped and undoped silicon can be estimated by assuming the thickness of the doped layer to be ca. 50 nm, and thus is over 1500:1. The threshold value for forming the masking layer is about 2×10^{16} ions cm^{-2}.

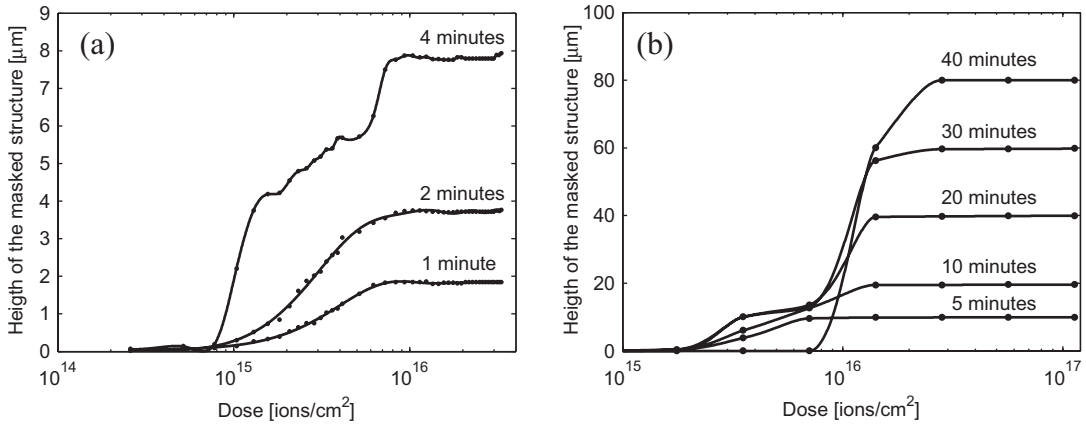

Figure 3.1: Obtained step height versus gallium dose for cryogenic ICP etching. Flattening of the curve corresponds to the etch-resistant mask. (a) fabrication of small structures, (b) fabrication of large structures. Different curves in the graphs represent the etching times.

The sloped edge of the curve on Figure 3.1(a) indicates that there is a region, where the gallium dose governs the resulting structure height enabling the fabrication of three dimensional structures. This assumption was tested by creating and etching a variable doping dose area. The results are shown in Figure 3.2. The shape of the obtained structure roughly followed the doping profile with some erosion on low doses and saturation at high doses.

Ga^+ doping dose for masking in TMAH

In publication VI the FIB induced gallium masking was characterized for wet TMAH etching. The method and the main results are similar to the ones obtained with cryogenic DRIE etching, except that required dose is about an order of magnitude lower when TMAH is considered, setting the threshold to 2×10^{15} ions cm^{-2} (Figure 3.3). Selectivity of the mask is 2000:1, which enables structures of 100 µm hight. The mask layer is assumed to be 50 nm in this case.

Maximum achievable resolution

After the proper masking dose was found, it became possible to move on to the resolution tests, where the minimum line width is determined. The approaches for TMAH and DRIE etching methods were slightly different, as DRIE enables fabrication of arbitrary patterns, but TMAH etching is limited by the crystallographic

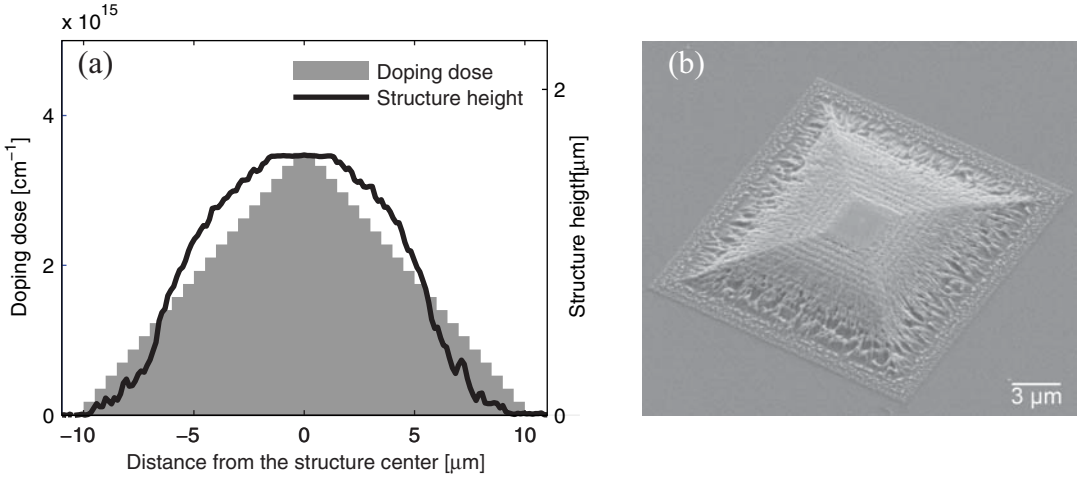

Figure 3.2: 3D structuring. (a) Ga^+ doping dose and the height of the resulting structure: dose steps and the corresponding structure profile measured by an atomic force microscope (AFM) after 1 min etch with cryogenic DRIE. (b) micrography of the resulting pyramid.

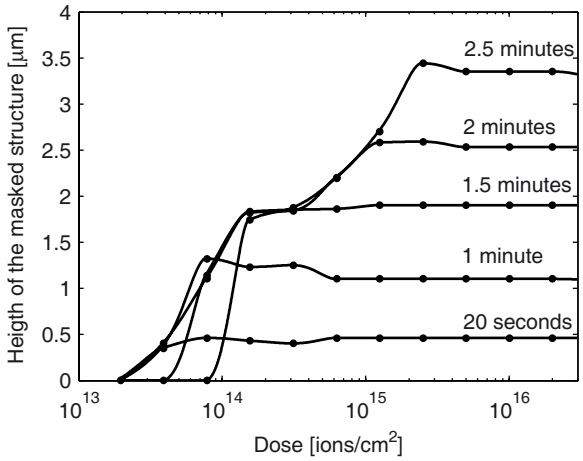

Figure 3.3: Obtained step height versus gallium dose for TMAH wet etching. Flattening of the curve corresponds to the etch-resistant mask.

nature.

For both methods the line pitch tests were performed and the results are shown in Figure 3.4. Each method was used to produce gratings with 20 lines μm^{-1}, however, in DRIE experiments, the doped lines became approximately 5 nm wider compared to the intended mask width, but in the case of TMAH etching, the lines became

narrower than projected by an amount of 10 nm.

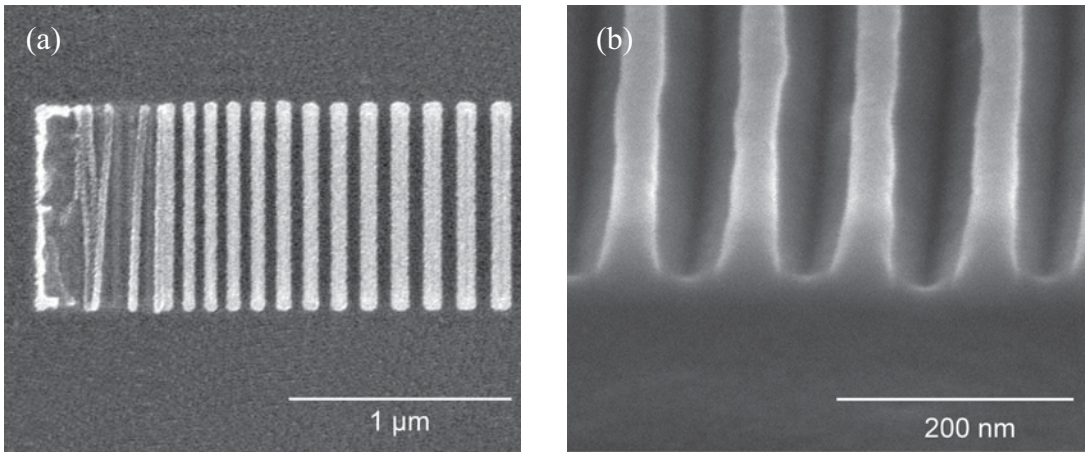

Figure 3.4: Line pitch tests (a) Cryogenic DRIE etching (minimum masked line 54 nm, pitch 100 nm), (b) TMAH etching (minimum masked line 40 nm, pitch 100 nm).

To find the ultimate limits for resolution, stand-alone structures were fabricated with both methods (Figure 3.5). It was possible to produce pillars with the FIB and DRIE processes, and the ones which are 40 nm in diameter and 600 nm high were obtained (Figure 3.5(a)). By the FIB and TMAH process, the fabrication of the pillars is not possible due to the limitations of the crystallographic etching. However, etching trenches with narrow, vertical walls between them is realizable. The width of the final structure was measured by taking a cross-section of such a structure (Figure 3.5(b)). The result was a 15 nm thick and 570 nm high vertical wall. Both of the structures have a visible doped masking layer on top of them. In case of TMAH etching, a triangular shape of the mask corresponds to the ion (and doping level) distribution inside silicon after the local implantation.

The masking is not limited to isolated structures, but can produce arbitrary shapes within the restrictions of the etching method in use. The repeatability of the masking is excellent; Figure 3.6 shows a matrix of 1296 identically masked pillars. The shape of the mask on top of each pillar is not perfectly round due to a slight misalignment of the ion beam, but all the masks have exactly the same shape. Pillars themselves are not etched completely evenly, as the outer rows, and especially the corner pillars have boundary conditions which differ from the boundary conditions for the pillars inside the matrix, which affects the DRIE process.

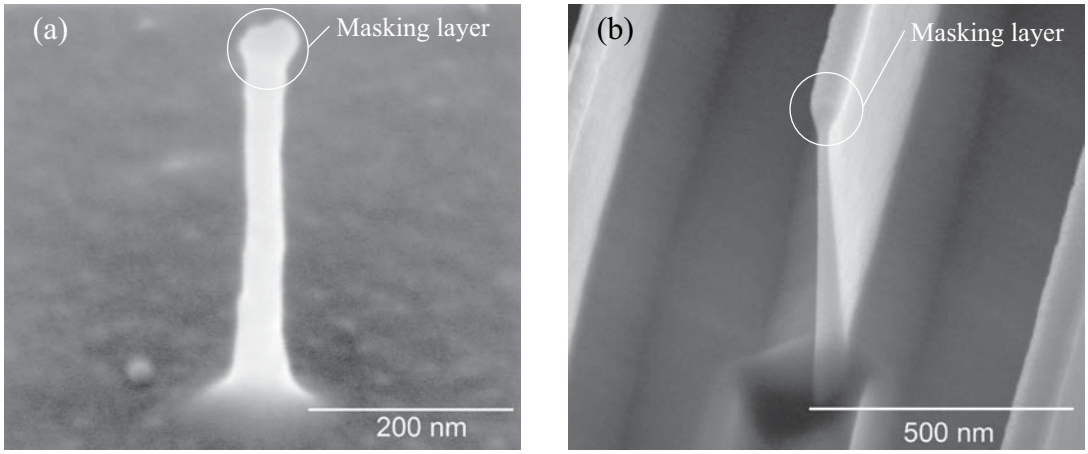

Figure 3.5: Single feature minimum size (a) For FIB and cryogenic DRIE process, pillar diameter is $d = 40$ nm ($h = 600$ nm), (b) for FIB and TMAH process vertical wall can be made $s = 15$ nm thick ($h = 570$ nm).

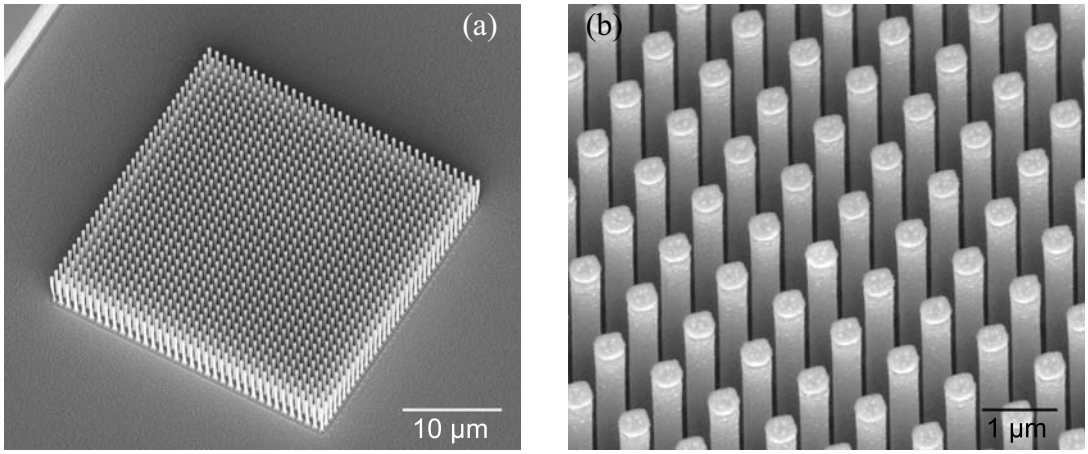

Figure 3.6: Masking repeatability test, a matrix of 36×36 dots was irradiated and pillars were etched in cryogenic DRIE, resulting in over 1000 identical structures. The diameter of the pillars is 350 nm and the height is 4 µm.

Alignment of doping regions

There are two different methods that can be used with SEM/FIB dual-beam machine to enable accurate alignment of the structures without alignment marks on the substrate. If the sample is flat, not tilted and conductive enough to neglect the charging effects, micron accuracy in positioning of exposure can be achieved by aligning electron and ion microscopes at the same spot on the sample. In this way

Writefield side [µm]	**Current [pA]**	**No mask [sec]**	**Full mask [min]**
500	22000	9.09	3.0
192	6500	4.55	1.5
125	2800	4.46	1.5
83	920	6.04	2.0
63	280	11.16	3.7
50	93	21.51	7.2
36	48	21.26	7.1
25	9.7	51.55	17.2
13	1.5	83.33	27.8

Table 3.1: Exposure times for masking (maximum ion contamination level with no mask formation: 5×10^{14} ions cm^{-2}, full mask level: 10^{16} ions cm^{-2}

navigating by the electron beam and exposing by the ion beam becomes possible. This method does not contaminate the processed area of the sample with ions and is suitable when delicate structures such as nanotubes or graphene must retain their properties during the exposure.

A much more accurate method is to use FIB for the alignment, as the ion microscope image shows exactly where the sample is going to be exposed and no misalignment between the electron and ion beams can take place. This method allows also tilted samples and even samples with pre-made height differences, so that pre-fabricated structures can easily be patterned. The limitation of the direct alignment with FIB is due to ion contamination, because the same ion beam is used for alignment and exposure. The current can not be reduced during alignment because switching currents degrades the alignment accuracy and the imaging time has to be kept short enough not to form a masking layer over the whole imaged area.

As can be seen from Figures 3.1 and 3.3, doses in below 5×10^{14} ions cm^{-2} for DRIE and below 5×10^{13} ions cm^{-2} for TMAH are not sufficient to form a masking layer. To calculate a corresponding imaging time, exposure current and area must be known. Table 3.1 shows some typical values for most used current/writefield combinations. The combinations were chosen so that the maximum writefield at each current would be available with the machine in use.

The data in the table reveals that it takes at least 4 seconds of continuous scanning with FIB to form a masking layer on a substrate. Using scan resolution of 512×512 pixels and dwell time of 100 ns, around 150 (DRIE) or 15 (TMAH) frames can be taken during this safe time. Usually, if SEM is used for rough alignment, only from three to five FIB frames are required to achieve the satisfactory results (Figure 3.7).

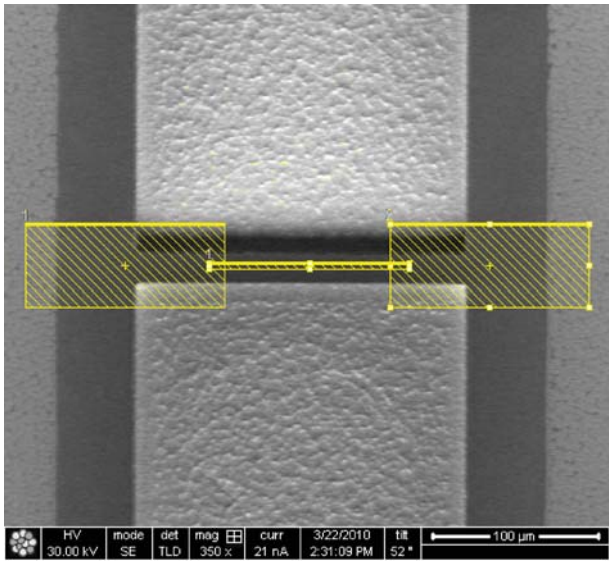

Figure 3.7: FIB image of the structure to be modified. Filled overlay rectangles indicate the areas to be doped by Ga^+ ions.

3.1.2 Suspended structures

Using the patterning technique described above it is also possible to create suspended structures by etching the silicon also beneath the doped layer. One way to achieve this is to change the etching mode in cryogenic DRIE to the crystallographic one, by decreasing the SF_6/O_2 - ratio, or by completely eliminating oxygen while still keeping the temperature of the sample at -120 °C (Figure 3.8(a)). As an alternative, wet etching can also be utilized (Figure 3.8(b)). In both cases the crystal and pattern orientations should be chosen according to the rules shown in Figure 2.9 to obtain proper undercut.

A somewhat simpler, but not that versatile method for releasing structures is isotropic etching. This mode can be obtained by etching the sample in pure SF_6 plasma at temperatures above -80 °C (Figure 3.9(a)).

The minimum feature size for the dense structures is about the same as in the case of standard etching, but single released bridges can be over etched resulting in partial consuming of the free standing Ga^+ rich layer. With the overetching technique, only the mechanical strength of the structures limits the achievable feature size. Using the cryogenic DRIE 20 nm wide bridges were obtained (Figure 3.9(a)), and for TMAH etching the corresponding value was 25 nm (Figure 3.9(b)).

The thickness of the resulting structures varies between 20 nm to 50 nm and is determined by the implantation depth of gallium ions, which depends mainly on

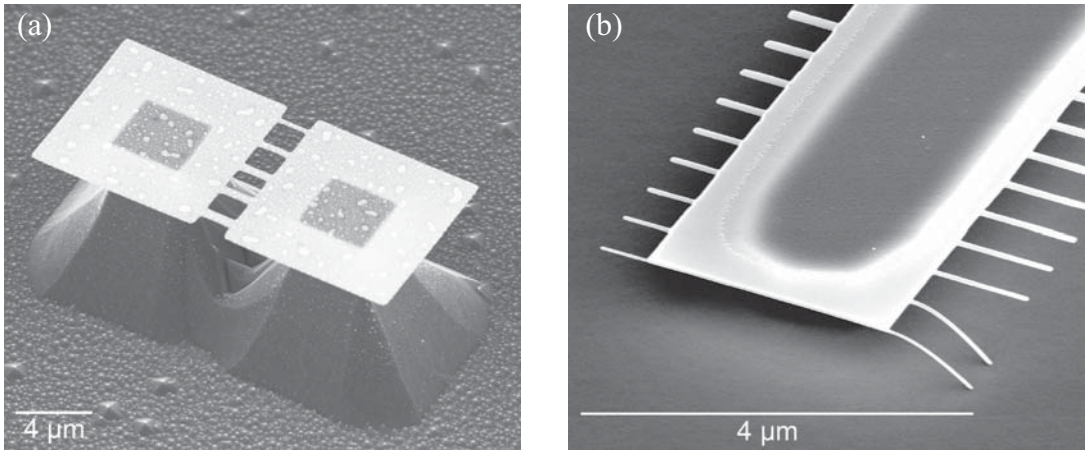

Figure 3.8: Fabrication of released structures on Si (111) substrates using crystallographic etching. (a) 1 µm to 100 nm wide, 2 µm long bridges with the implantation dose of 4×10^{16} ions cm^{-2} released in cryogenic DRIE, (b) 500 nm long and down to 35 nm wide beams with the implantation dose of 4×10^{15} ions cm^{-2} released in TMAH.

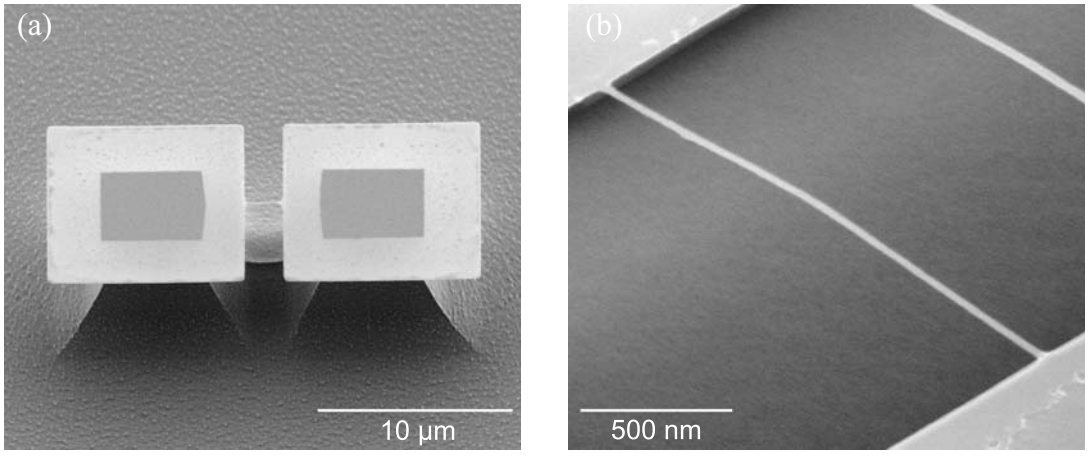

Figure 3.9: (a) Structure released by FIB-DRIE using isotropic etching. The undercut lines are smooth and round contrary to Figure 3.8(a) where edges and crystal planes are visible. The bridge dimensions are: length 2 µm, width < 20 nm, thickness < 30 nm. (b) 2 µm long and 25 nm wide bridge released by TMAH etching.

the acceleration voltage and less on the dose implanted. The dose affects the final thickness of the components mainly through the sputtering effect. This issue is described in more detail in Ref. [22].

3.2 MEMS Fabrication methods

Fabricating functional micromechanical structures can be a long, multistep project, which may take several months, if proper stability and encapsulation are also required [41]. In this work we concentrate on obtaining components of acceptable quality are rapidly using only one mask level.

The basic fabrication method is quite straightforward as shown in Figure 3.10. A designed pattern is transferred to a mask on top of a SOI (Silicon On Insulator) wafer in a first step. In a second step the pattern is replicated into device layer of SOI using cryogenic DRIE. Because of severe overetching during the step 3, notching occurs and releases the moving parts of the system [42, 43, 44].

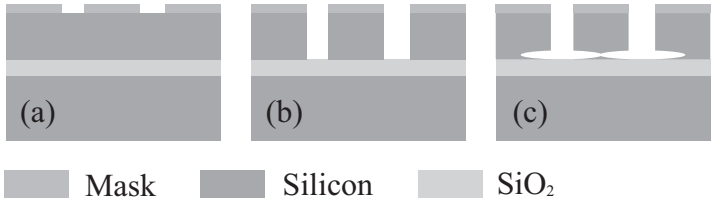

Figure 3.10: Notching-based MEMS fabrication process. (a) exposure of the masking layer, (b) etching through the device layer, (c) overetching and notching.

Even though this process is simple to realize, the component should be carefully designed in order to induce notching at appropriate locations. Also a high durability of the etching mask is needed to allow overetching without failures. The mask durability issue is most essential, when thin photoresists must be used because of the small feature sizes.

3.2.1 Alumina hard mask process

Process description

In Publication II we report on utilizing ALD grown Al_2O_3 layer as a hard mask for the EBL pattern. EBL was performed on PMMA electron sensitive resist, which has many good qualities, as robustness, high resolution and simple development but has poor resistance against etchants. A conventional hard-mask approach was utilized to resolve the issue. The novelty of the approach is in the the exceptional properties of the hard mask which can be patterned even through PMMA and at the same time withstands all the subsequent etching steps. (Figure 3.11).

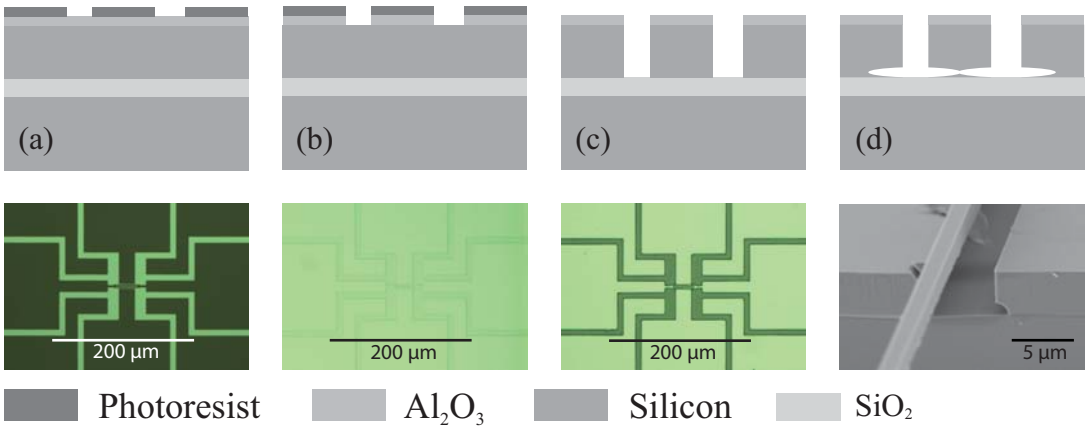

Figure 3.11: EBL process using the Al_2O_3 hard mask. (a) Hard mask deposition on SOI wafer using ALD, resist (PMMA) spinning, exposure and development, (b) hard mask etching (RIE, argon milling), (c) silicon etching by Cryo-DRIE, (d) over-etching to achieve release by notching.

As a substrate was chosen an SOI wafer with 4 µm thick device layer doped with boron to 0.02 Ohm·cm and having 200 nm buried oxide layer. The low resistively silicon makes it possible to omit metalization of electrodes without causing too high losses for the electrical signal levels.

After pre-cutting and cleaning (with acetone and isopropanol (ACE/IPA), silicon chips 6×6 mm^2 in size were coated by alumina with a Beneq TFS 500 reactor using H_2O+TMA (trimethylaluminium) chemistry at 220 °C. Only 40 cycles were deposited yielding the layer thickness of 4.5 nm. The excellent resistance of Al_2O_3 in cryogenic DRIE [26], enables the masking layer to withstand etching for more than 2 hours, producing structures over 250 µm high at silicon etch rate of 2 µm/min. Because in this process the etching time did not exceed 15 minutes, the layer durability was more than sufficient. Even thinner layers could have been used, as in ALD a pin-hole free film is formed already after 10 cycles (equaling 1 nm in thickness [45]), but in practice very thin layer scratches easily, so that extra alumina adds to the robustness of the process.

A solution of 2% PMMA in anisole was spun on the chips at 4000 rpm resulting in a film of 82 nm in thickness after 10 min pre-baking at 170 °C. Then EBL was performed with a current of 130 pA (corresponds to 20 µm aperture). The machine used was a Zeiss Supra 40 electron microscope with an external Raith ELPHY Quantum pattern generator. The exposition dose was set to 200 µC/cm^2 and the development was done in IPA/H_2O solution (90 % / 10 %) for 45 seconds (Figure 3.11(a)).

	Step	Tool	Time	Level	Comment
1	Wafer dicing	Dicing saw	1 h	Wafer	Wet
2	Cleaning	ACE/IPA	1 h	Wafer	Wet
3	Al_2O_3 deposition	ALD	2 h	Wafer	Dry
4	Resist spinning	Spinner/Hot plate	0.5 h	Chip	Wet
5	Lithography	EBL	1-3 h	Chip	Dry
6	Development	IPA/H_2O	0.5 h	Chip	Wet
7	Hard mask etching	RIE	0.5 h	Chip	Dry
8	Silicon etching	Cryo DRIE	0.5 h	Chip	Dry
9	Bonding	Wire bonder	0.5 h	Chip	Dry

Table 3.2: MEMS fabrication process flow using EBL and Al_2O_3 hard mask

The next step is to transfer the written pattern in the resist to the alumina layer, which is done using conventional reactive ion etching (RIE). SF_6 plasma has been used for similar applications [46] achieving the etch rate of 5 nm/min, but for a 4 nm thick layer simple argon milling is sufficient. Being chemically passive argon plasma has a low etching rate for polymers, so the timing restrictions are loose in estimating the etch duration. Several tests have been made with Oxford Plasmalab 80 RIE equipment and with 250 W power, 10 mBar pressure, 40 sccm argon flow etch rate of 7 nm/min was achieved for alumina. At the same time PMMA was consumed with a rate of about 5 nm/min and extra 32 nm were etched during the plasma ignition. The sample was etched in argon plasma for 2 minutes consuming half of the mask thickness but this time was enough to ensure that the alumina layer was totally etched away (Figure 3.11(b)).

The final step, where the silicon structures are defined, was performed in Oxford Plasmalab 100 cryogenic DRIE using SF_6/O_2 chemistry (40 sccm and 6 sccm respectively), pressure of 10 mTorr, temperature of -110 °C, 3 W forward power and 1000 W ICP power. The time was varied to achieve the optimal notching. Etching for approximately 8 minutes was found to produce the optimal result (Figures 3.11(c-d)).

After etching all mask layers (in this case PMMA resist and Al_2O_3 hard mask) should be removed, but because the resist is readily etched away during the DRIE step, and the hard mask is so thin, that it does not severely interfere with the functionality of the devices, all the removal steps can be omitted. All what is still left to do is packaging and bonding (Figure 3.12). The use of ultrasonic aluminum wire bonder allows to bond wires directly to silicon, so that no metallic bonding pads are needed. For a better contact, the chips can be sintered on a hotplate at 425 °C for 30 seconds.

As can be seen from Table 3.2, there are three wafer-level steps and 6 chip level

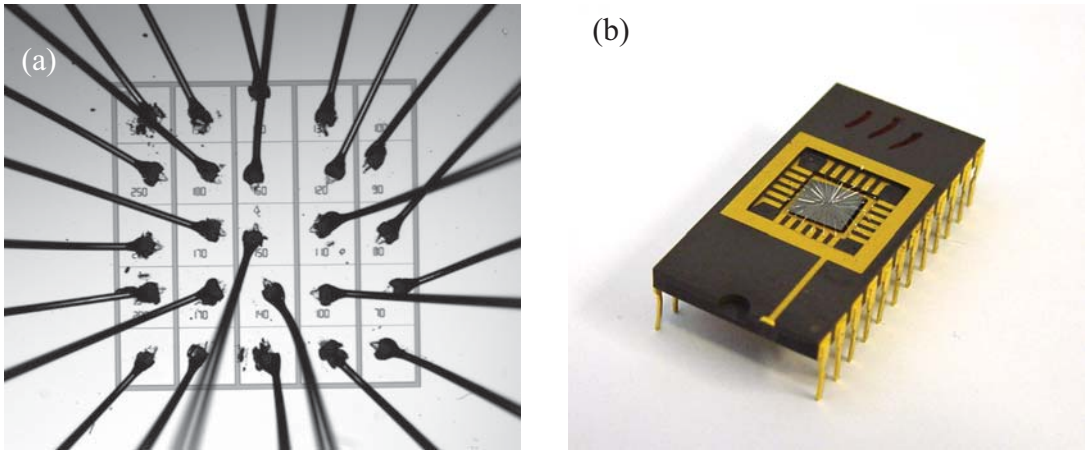

Figure 3.12: (a) Test component with aluminum wire bondings to plain silicon, (b) packaged and bonded component.

steps in the process. Wafer level steps take up to 4 hours, but result in producing several (up to 200) chips. Steps 4 to 9 should be done separately for each chip or groups of chips every time the component design is changed, but all the chip-level steps from applying the resist to packaging take only about 3.5 - 5.5 hours, including all the other tasks (such as pumping times of the machines).

The major time consuming step on the chip level is EBL, which takes a couple of hours depending on the required resolution, on the number and on the complexity of the exposed components. It is quite hard to speed up this part of the process without loosing in quality.

There are several wet processing steps, where the samples are submerged into liquid. Wafer dicing and cleaning do not affect the final result too much, but resist spinning and development require extra care. Especially the reproducibility makes up a clear challenge, this issue will be addressed in the next chapter.

Achieved results

Using the described technique, test structures were fabricated to determine the design rules for the mask drawing. The MEMS resonators were designed using the discovered rules and fabricated to prove the feasibility of the process.

There is only one restriction concerning the design of the component that is released utilizing the notching effect; the structures have to have surrounding trenches that are of certain width in order to be released. Also care should be taken not to

accidentally release any additional structures. Figure 3.13 shows the results of a test run performed for a device layer thickness $h = 4$ µm, the etch time was $t = 16$ min, which corresponds to 32 µm etch depth if no buried oxide or RIE lag are present.

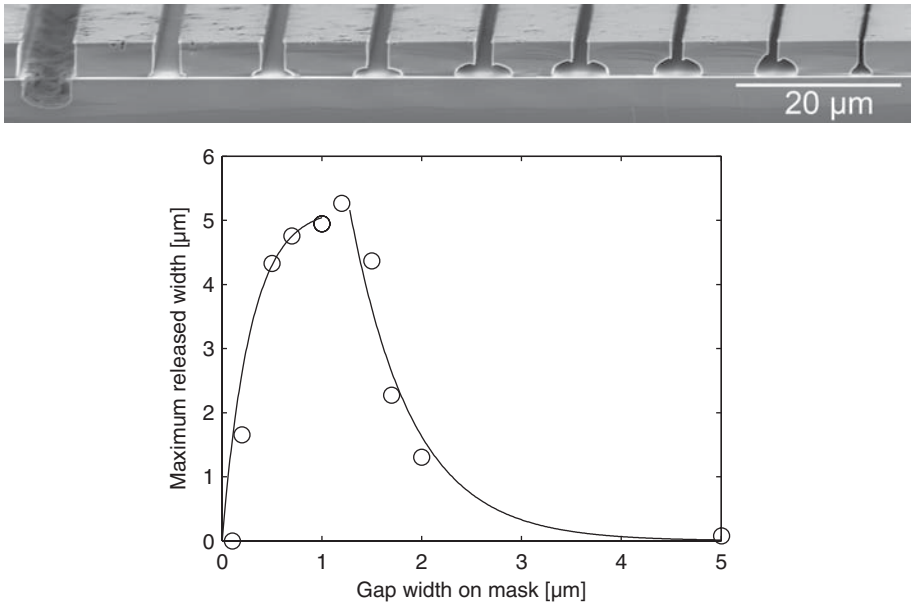

Figure 3.13: Analysis of notching. The upper image shows a cross-section of a variable width ($w = 5$ µm to 0.2 µm) trench pattern. In the lower graph the extent of notching (widening of the trenches) is plotted as a function trench width. The continuous lines serve as a guide to the eye.

The graph shows, that up to 5 µm wide structures can be released with an optimal gap width of ca. 1 µm. Wider gaps exhibit less notching, and narrower ones suffer from the RIE lag. If required, wider structures can be released with narrow gaps by increasing the etching time. However the durability of the buried oxide has to be sufficient to withstand long etch times, which was not the case with the first trench in a test run described above.

The fabrication method was tested by etching micromechanical high-frequency resonators. A double-ended tuning fork resonator (DETF) with the branch length $l = 38$ µm, width $w = 2.5$ µm and the coupling gap width $d = 1$ µm was fabricated and characterized. The resulted proper electrical response from the component ensured the suitability of the process for RF-MEMS applications (Figure 3.14).

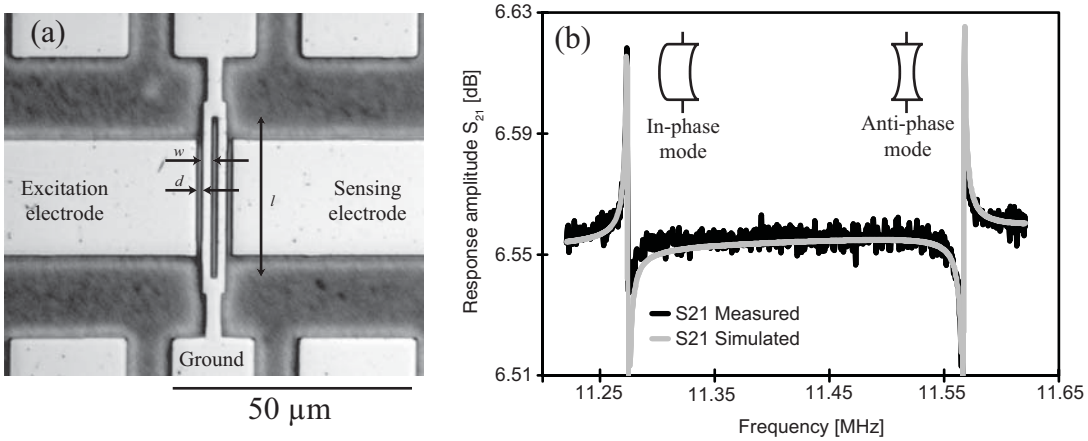

Figure 3.14: Optical image of an RF-MEMS resonator fabricated using alumina hard mask process and the corresponding electrical transmission (S_{21}) measurement result as a function of frequency in the vicinity of the mechanical resonances. At the first resonance the vertical beams move between the electrodes in-phase, and at the second - in anti-phase. The dimensions are: beam length $l = 38$ µm, width $w = 2.5$ µm and the coupling gap width $d = 1$ µm.

3.2.2 Combined FIB-DRIE fabrication process

Gallium implantation masking process developed primarily for nanostructure fabrication can easily be scaled up for producing microcomponents such as MEMS resonators (Publication V). The process utilizes the same notching effect as the hard mask process described above, but patterning is much simpler so the whole fabrication cycle consists of only two dry steps.

Process description

MEMS fabrication process using Ga^+ implantation as an etch mask starts by dicing an SOI wafer and cleaning the chips. In the case that is described in Publication V, a p-type boron doped to 0.01-0.02 Ohm·cm SOI wafer was used. The device layer thickness of the wafer was chosen to be 10 µm with 1 µm thick buried oxide (BOX) layer and 380 µm handle layer.

Because the doped Ga^+-layer itself has an adequate selectivity towards silicon during etching, no hard mask layers are needed, but the chips can be directly patterned by local FIB doping. A safe dose to start with is about 2×10^{16} ions cm^{-2}, but depending on geometry, size of the component and writing current, dose may have to be adjusted by a factor of four. Overexposing was not found to inflict severe

negative effects on the final structures, but the dose optimization is worth doing anyway as it directly decreases the total exposure time. The dose required for FIB to form a masking layer is an order of magnitude higher than the dose which is needed for EBL to expose the resist.

The treated area of silicon provides enough contrast under electron and ion microscopes (Figure 3.15(a)) and it is possible to precisely align more than one mask layer without dedicated alignment marks. Aligning the masks is required in such a case, where there is a considerable size difference between the individual features. In micromechanics such features are for example bonding pads and the moving parts. Bonding pads and connecting wires can quickly be drawn at the maximum current, and the mechanical device is exposed at larger magnification and smaller current to gain the required accuracy (see also Figure 2.3). Figure 3.15(b) shows the complete component after etching and Figure 3.15(c) demonstrates the accuracy of the alignment. Also note, that while at the overlaps of the conductive wires and the component, the Ga^+ dose is doubled and no signs of quality degradation are visible.

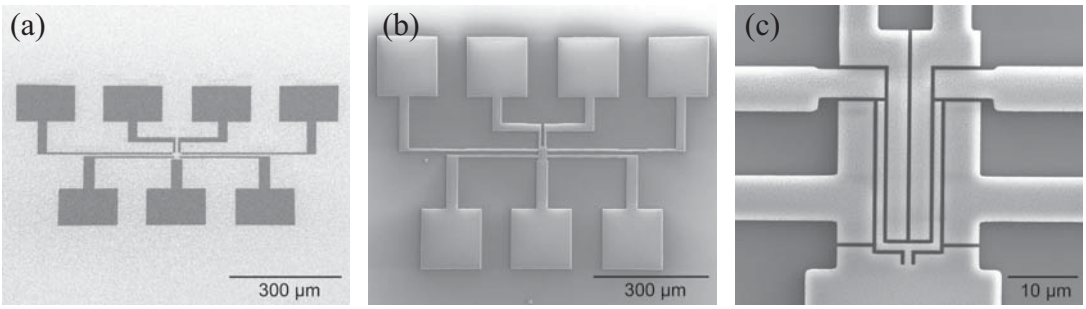

Figure 3.15: MEMS fabrication by FIBdoping and consequent cryogenic DRIE. (a) Ga^+ doped areas are clearly visible under the electron microscope enabling the alignment. (b) overall image of the component with bonding pads. (c) close up on the mechanical moving part of the resonator.

The exposed chips are etched in cryogenic DRIE as described above, and after etching the components are ready to be wirebonded and characterized.

As Table 3.3, which summarizes the MEMS fabrication process using Ga^+ doping, illustrates: the only wet processes (dicing and cleaning) are at the very beginning of the cycle, and applied at the wafer level. All the actual fabrication steps are dry, and depending on the complexity of the exposed devices, the whole fabrication cycle including packaging takes only from 2 to 4 hours.

	Step	Tool	Time	Level	Comment
1	Wafer dicing	Dicing saw	1 h	Wafer	Wet
2	Cleaning	ACE/IPA	1 h	Wafer	Wet
3	FIB patterning	FIB	1-3 h	Chip	Dry
4	Silicon etching	Cryo DRIE	0.5 h	Chip	Dry
5	Bonding	Wire bonder	0.5 h	Chip	Dry

Table 3.3: MEMS fabrication process flow using FIB Ga^+ masking.

Achieved results

The results of the FIB-DRIE process differs very little from the ones obtained by ALD-enhanced electron beam lithography process as the resolution and masking capability are roughly the same. As is the case with EBL on the Al_2O_3 mask, the double-ended tuning fork (DETF) test component, as expected, exhibits both in-phase and out-of-phase resonances (Figure 3.16).

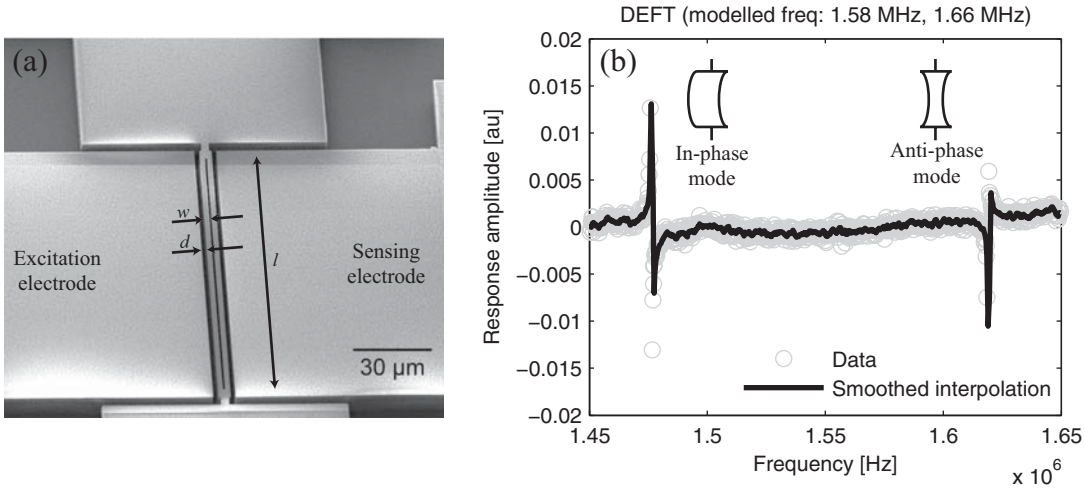

Figure 3.16: (a) An overview of an RF-MEMS resonator (beam length $l = 100$ µm, width $w = 2$ µm and the coupling gap width $d = 2$ µm) fabricated using FIB doping process. (b) The measured electrical transmission (S_{21}) indicating that both the in-phase and the anti-phase modes are excited.

Patterning method	Dose required (µ m^{-2})
EBL	10^{14} to 5×10^{15} *
FIB/DRIE	2×10^{16}
FIB/TMAH	10^{15}

* Depending on resist and acceleration voltage

Table 3.4: Exposure doses for various processes.

3.2.3 Comparing EBL and FIB patterning processes

For MEMS fabrication, ALD-enhanced EBL and FIB masking are equally suitable. When the height of the structures exceeds 2 µm, limited aspect ratio of cryogenic DRIE constrains the minimum feature size as long as the resolution of the mask is better than 50 nm. Such a resolution is achieved by both of the masking methods. There are, however, a few differences which affect the selection of the process.

EBL is a mature technique, and a huge variety of instruments are available. Also wafer-level exposure and accurate write field stitching are routinely performed. FIB, on the other hand, is much more an analysis and prototyping, than a standard fabrication equipment and is suitable to process only a few components at a time. Also electron beam photoresist exposure is inherently a faster process than FIB masking (Table 3.4) as up to 100 times smaller dose is required for exposure, so for bigger prototyping batches, as well as for a small-scale production, EBL is the patterning method of choice.

The downsides of EBL become evident, when considering fabrication of a few components and analyzing the process as a whole (Figure 3.17). EBL requires a hard mask to be deposited and patterned, as well as applying and developing photoresist. Compared to the single-step FIB masking - method, the extra steps of EBL are consuming a lot of time, but more importantly, resist-related steps are wet, which is acceptable as long as the wafer-level processing is concerned, but is a real challenge in chip-level processing.

3.2.4 Combining optical lithography and FIB masking

One obvious advantage of FIB masking is that it does not require any kind of resist applied on a structure before patterning. Together with dry etching this property enables patterning of existing 3-dimensional structures, which is virtually impossible by any other means. Modifying existing structures by this method is not significantly different from making structures from the very beginning.

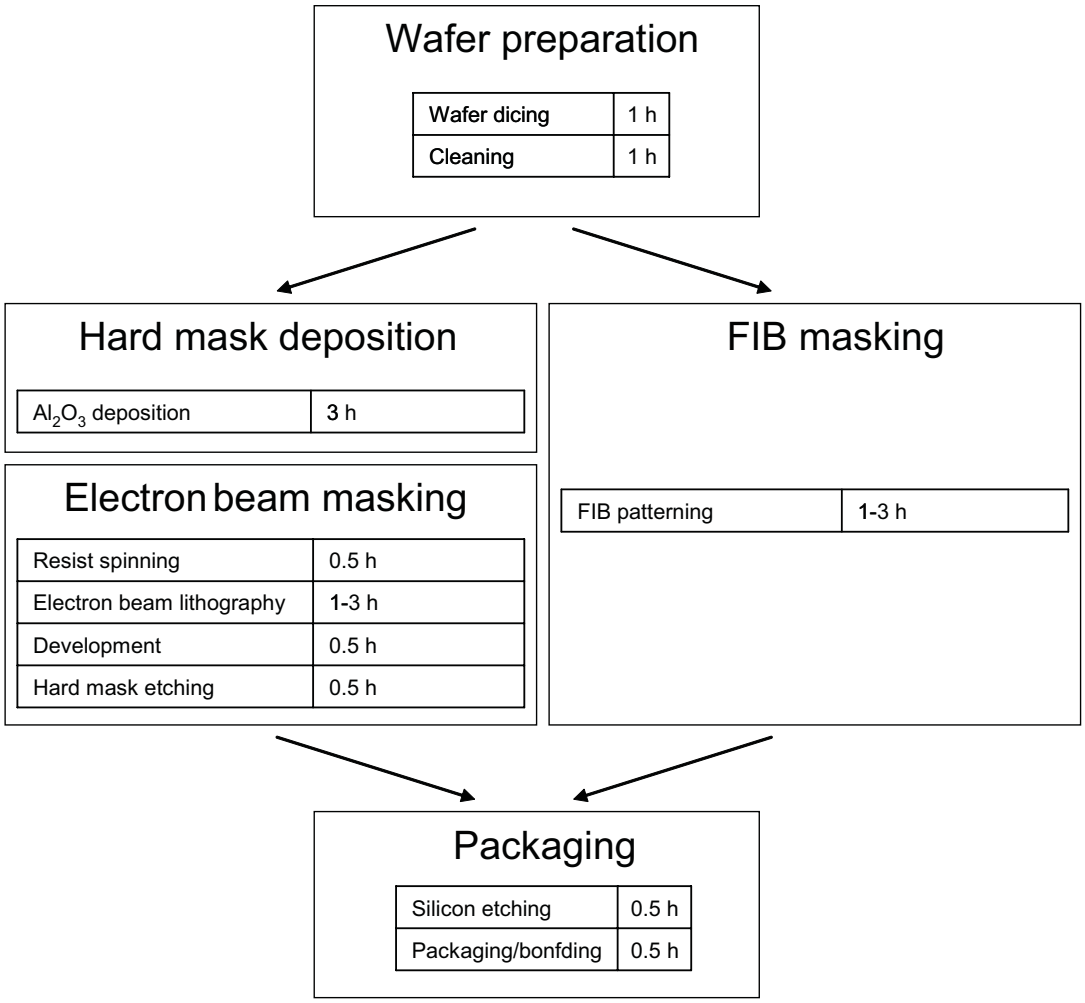

Figure 3.17: Process flow for EBL and FIB masking.

To demonstrate the alignment and modification possibilities for 3D structures, thermal actuators described in Ref. [47] were modified (Figure 3.18).

As a result, 200-µm long, 25-µm wide and 4-µm thick bridges were successfully narrowed down to 0.36 µm, which is beyond optical lithography limits and extremely hard to achieve with conventional FIB milling.

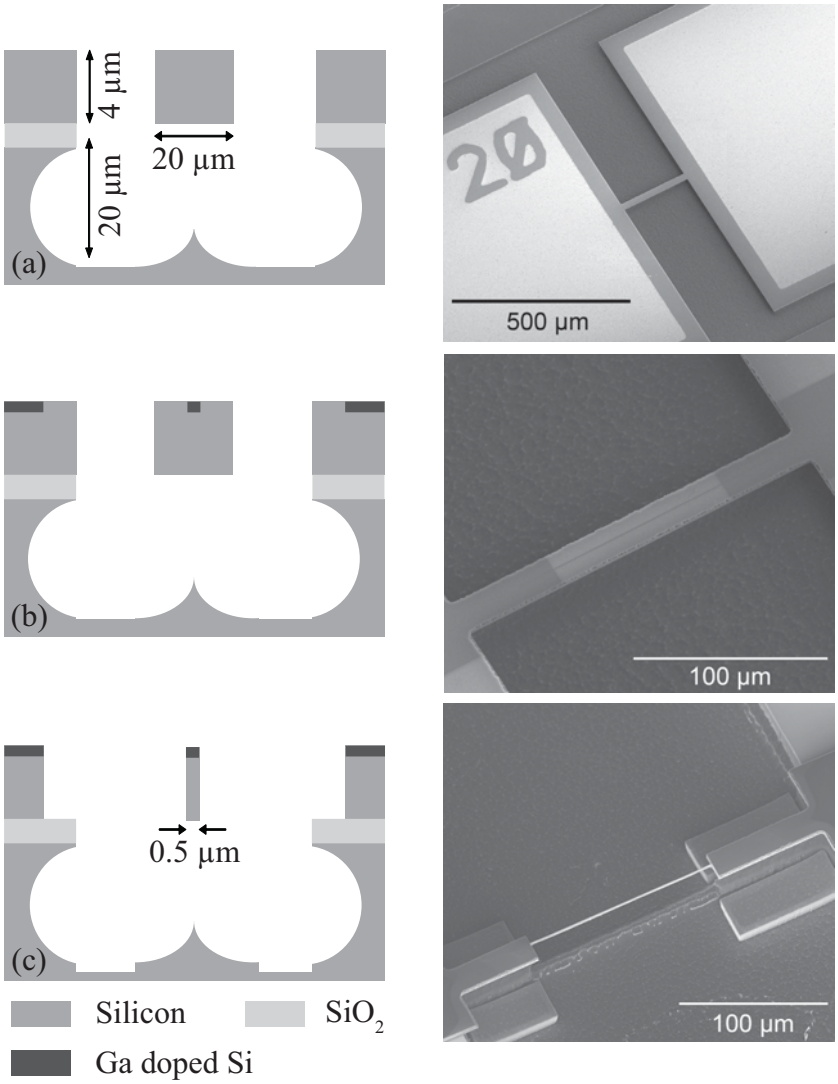

Figure 3.18: 3D device modification. (a) initial actuator prior to modification (200 µm × 25 µm × 4 µm), (b) masking layer is implanted by FIB, (c) the final structure is etched in cryogenic ICP etcher to the measures 100 µm × 0.36 µm × 4 µm.

3.3 ALD deposited alumina as an insulator

ALD deposited materials are virtually pin-hole free [45], which was utilized during the work described in Publication VII. The goal was to create a change in the environment in tunnel junction experiments. Silicon or oxidized silicon is often used as a substrate for tunnel junctions. In this approach, when the system is refrigerated to temperatures near absolute zero, silicon, no matter how strongly doped, becomes non-conductive. Adding a conducting, or superconducting, plane between

the junction structures and the substrate proved to severely decrease the electrical noise levels by capacitive shunting in metal-insulator-superconductor (NIS) junction and superconductor-insulator-metal-insulator-superconductor (SINIS) turnstile measurements (Publication VII).

3.4 Mechanics design and simulation

In Publication I the goal was to design a mechanical component, which has vibrational mode where the movement of one of the surfaces is exactly orthogonal to that surface without any tilting and is possible to realize with existing double-sided wet etching process [48, 49]. The simplest implementation of such a component is a round membrane with a mirror glued at its center, vibration of the membrane would ideally move the mirror but not tilt it. The weaknesses of such structures are in challenging fabrication and in a resulted low quality factor.

Good quality factor non-tilting out-of-plane mode resonators can replace torsional resonators and give a final advantage in pursuit for measuring a standard quantum limit for optical detection [50]. Torsional motion of the resonators degrade interferometers performance when used as one of the mirrors. Non-tilting out-of-plane resonators do not have such disadvantage [51].

The obtained component is easy to fabricate, has two parallel mirror surfaces moving in anti-phase at frequency $f = 26526$ Hz and has a quality factor of $Q = 100000$ at room temperature and at pressure $p = 10^{-3}$ mbar. Those parameters were achieved by combining torsional mode vibrations known to produce high quality factors [52] with a frequency-matched clamping and large out-of-plane motion of the beam (Figure 3.19).

The component consists of a central beam with dimensions 1.5 mm $\times$ 14 mm $\times$ 0.38 mm. This beam is mainly responsible for the resonance frequency of the whole structure and is driven in its second eigenmode so that there are 3 nodes and 2 antinodes present (Figure 3.20).

The antinodes are used to mount the square vanes (0.8 mm $\times$ 0.8 mm $\times$ 0.38 mm.), which act as non-tilting mirrors. Each vane is mounted to the beam by support anchors of minimum width available in the process (ca. 75 µm). The openings, which are made in the beam to allow the vanes to move freely, modify the resonant frequency of the whole structure and affect the position of the anti-nodes. Because of this, positioning of the vanes and their openings had to be carefully iterated. As the anti-nodes virtually have no torsional movement, the vanes stay parallel to the original component plane during all the phases of vibration (Figure 3.21). The optimization of the structure was done using commercial finite element modeling (FEM) software ANSYS.

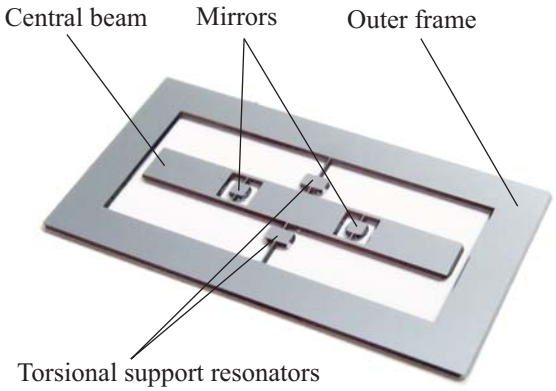

Figure 3.19: Out-of-plane mode high-Q silicon oscillator. The size of the outer frame is 21 mm × 11 mm. Central beam is 1.5 mm × 14 mm, the mirrors - 800 µm × 800 µm and the connecting bridges are 75 µm wide. The thickness of the component is 380 µm.

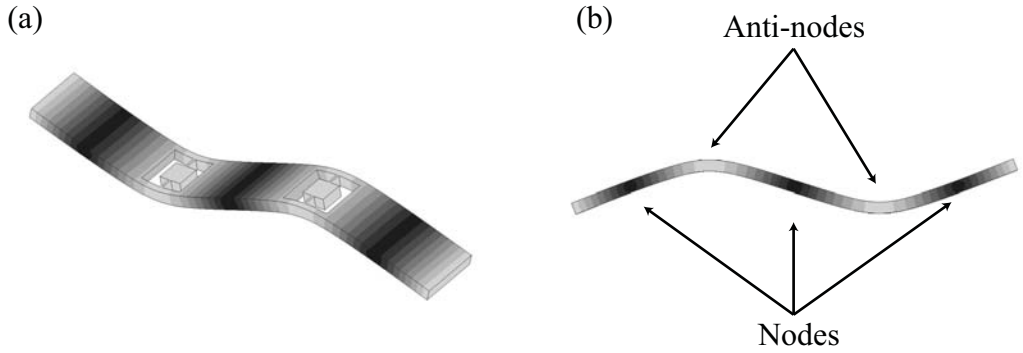

Figure 3.20: Central beam vibrating in the second eigenmode.

To achieve low energy dissipation and high quality factor, the beam is anchored to the outer support frame by the center node from the two sides by torsional resonators (Figure 3.22). The anchors have the resonance frequency matched to the beam. This anchoring scheme matches the impedances of the vibrations [53, 54] effectively de-coupling the center beam from the frame. To increase robustness, extra weight is added to the supporting beams, to bring their resonance frequency down to the frequency of the center beam. Alternatively the matching could be performed by simply making a sufficiently long support beam, but in case of cm-scale low frequency components, such scheme is not practical as the beam length would be longer than 18 mm. With a ballast weight, the same 75 µm wide bridge

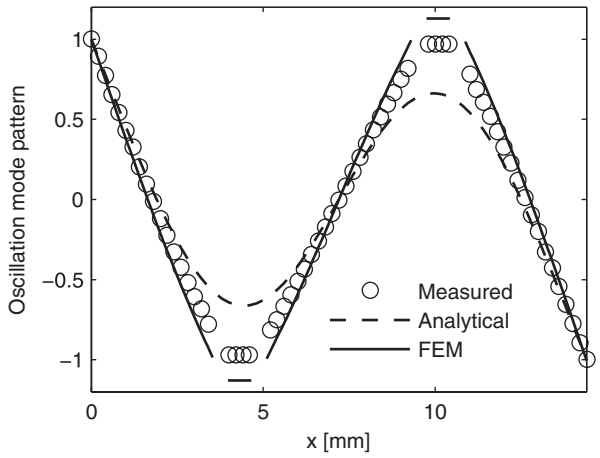

Figure 3.21: Comparison between measured vibration mode, analytical and FEM models.

can be made only 2.5 mm long, which is still mechanically robust.

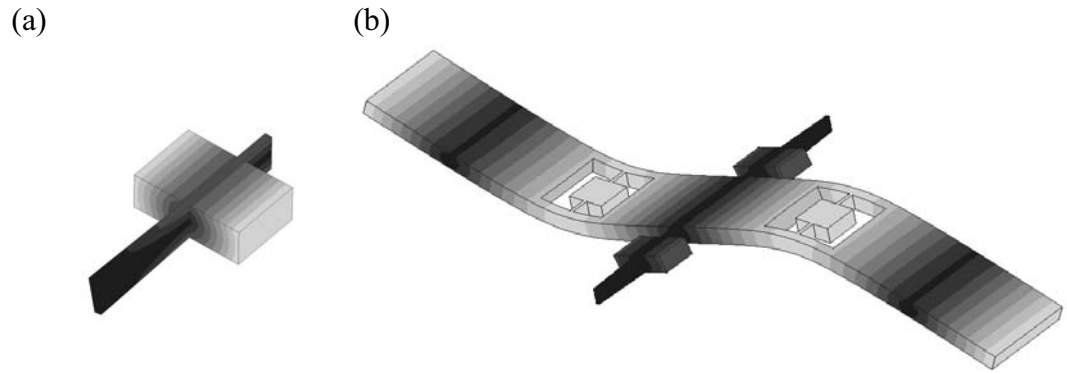

Figure 3.22: Resonator clamping by frequency-matched torsional supports. (a) support with a torsional spring and a counterweight, (b) resonator beam with supports attached.

The measurement results show, that the component performs as designed, exhibiting $Q = 100000$ at $f = 26.8$ kHz and $p < 10^{-2}$ mBar. The oscillation amplitude of the vanes was measured to be 10 nm and the tilt of the vanes induces at most only 100 pm difference between measurements across the vane indicating that the in-plane motion is achieved and the tilt of the vanes is ca. 0.1 µrad.

4 Summary and outlook

The main results of this thesis are related to the development of various fabrication techniques for structures that contain sub-micrometer size features with high aspect ratio. The developed procedures can be performed in a fraction of time compared with conventional techniques without leading to deteriorated quality.

In publication I a new type of component with a non-tilting-out-of-plane mode of vibration was developed. The design was finalized by utilizing FEM modeling. The measurement results show good consistency between simulations and fabricated structure operation. High quality factor of Q > 100 000 in vacuum and low tilting of the mirror vanes (ca. 0.1 µrad) were achieved. Those properties can be utilized in experiments where movement of parallel surfaces is important. In addition to interferometric applications, non-tilting-out-of-plane vibrational mode components can be used in scanning probe applications.

In publications II and VII ALD deposited aluminum oxide was utilized for two different purposes. In publication II the material was used as an etching mask, to achieve a reliable pattern transfer from a 100 nm thick EBL photoresist to 4 µm silicon structures. In publication VII aluminum oxide was used as a high-quality insulator in the experiment, where capacitive shunting of NIS junction is shown to decrease the subgap leakage by an order of magnitude by protecting it from photon assisted tunneling.

A novel masking method for cryogenic deep reactive ion etching is presented in publication III. The masking properties of the FIB Ga^+ implanted silicon are investigated and the resolution tests are performed. Using the doping dose in the order of 10^{16} ions cm^{-2} (equivalent of milling of 3 - 7 nm of material) selectivity of 1:1000 to the non-treated silicon and feature sizes as small as 40 nm were achieved. The method greatly simplifies the fabrication process of micro- and nanostructures enabling the transfer of arbitrary patterns to silicon in a matter of hours. Comparing to conventional FIB processing, the proposed technique is orders of magnitude faster and produces a better quality side walls due to a separate etching step. This technique was extended in publication IV to produce free-standing structures that are ca. 30 nm thick composed out of Ga-rich silicon, which is undercut in the etching step by using crystallographic or isotropic modes.

Experiments similar to the ones reported in publications III and IV were conducted with TMAH wet etchant in publication VI. The results showed that the resolution achievable by the FIB masking did not significantly change, but the ion dose required to form the protective layer is smaller by an order of magnitude. Anisotropic wet etching can not produce arbitrary features due to dependence of the etched shapes from the crystal orientation, but on the other hand, when the structures are properly

designed, almost ideally vertical, smooth walls with huge aspect ratios are easily achievable, as well as sloped structures.

Finally, in publication V FIB implantation and cryogenic DRIE etching are shown to be a viable combination for MEMS manufacturing. Two types of systems were produced: electrothermal actuators and microelectromechanical MHz - range RF resonators. In the first case 3D structures made by optical lithography and DRIE etching were modified by the FIB-DRIE method. The width of the final devices was beyond optical contact lithography limits (< 400 nm), nevertheless they performed consistently compared with non-modified components. Also the alignment to the predefined structures was introduced for sub-micron features. The released RF-MEMS test components were fabricated and tested to produce both the resonances predicted by simulations, which show that the notching effect used for the component release performs adequately not only with the hard mask, as shown in publication II but also with the gallium dopant masking in all-dry processes.

The future prospects for the work can be divided into three branches. The first branch is in the further process development and improving the resolution and accuracy of the maskless patterning techniques by the similar methods which are used in electron beam lithography. Another direction is to extend gallium doping masking technique from silicon to other materials.

The second branch is in developing released micro and nanomechanical system based on the developed fabrication processes. A quick turnover time makes it possible to produce several generations of the components in the same time it takes to produce the first generation for the conventional techniques. Additionally, high uniformity of the process enables fabrication of complex systems containing thousands of coupled active components.

The third open direction is in the fields of photonics and plasmonics. With the ability to fabricate three dimensional silicon structures with the precision of tens of nanometers it is possible to construct confined two dimensional photonic crystals. Especially when plasmonics is concerned, interesting phenomena have been predicted theoretically, but the theories lack the experimental validation.

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